

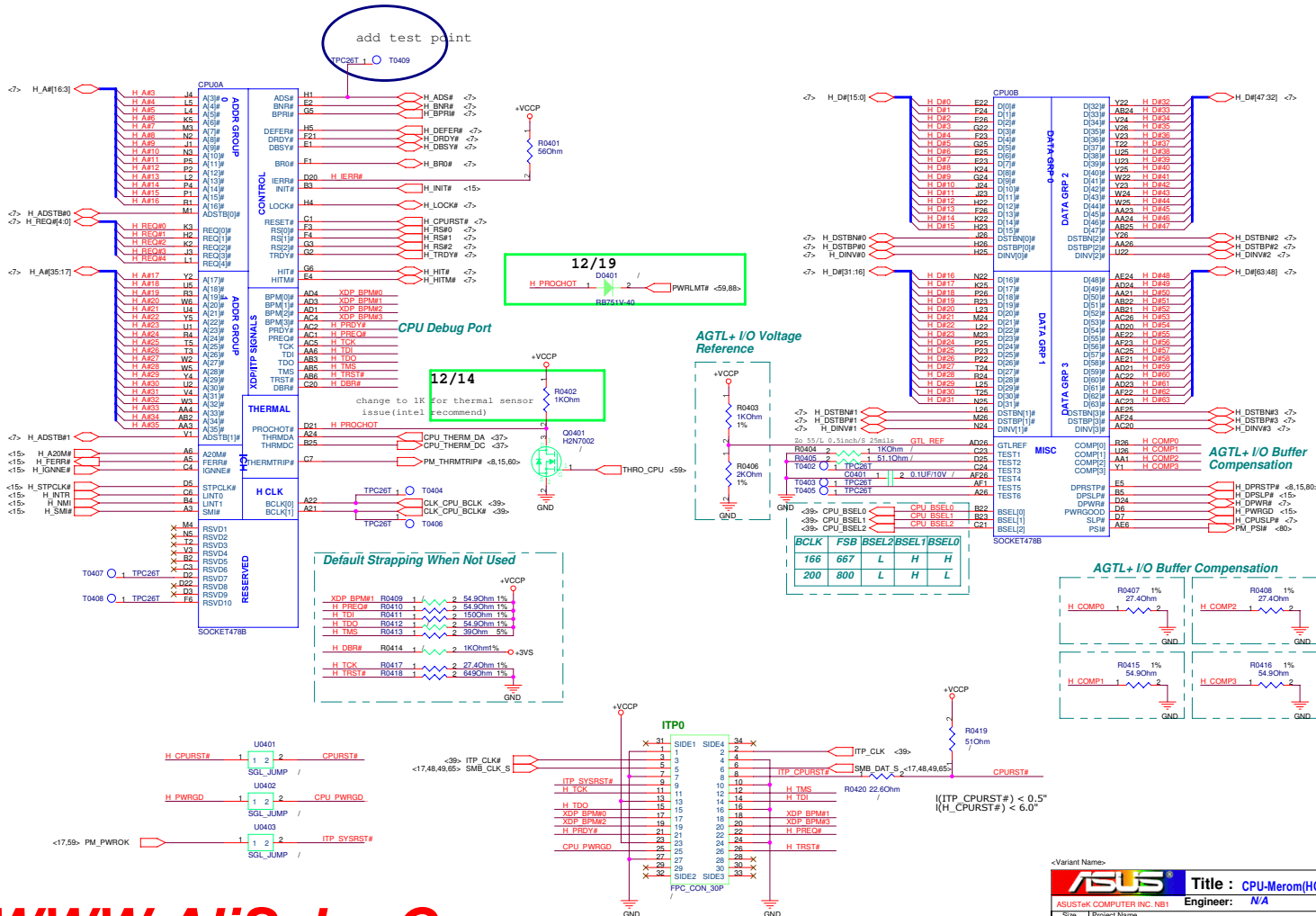
## EC\_IT8511TE SETTING

Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	LCD_BL_PWM	O
33	PWM1/GPA1	FAN_PWM	O
36	PWM2/GPA2	/	
37	PWM3/GPA3	/	
38	PWM4/GPA4	CHG_LED_UP#	O
39	PWM5/GPA5	PWR_LED_UP#	O
40	PWM6/GPA6	/	
43	PWM7/GPA7	LCD_BACKOFF#	O
153	RXD/GPB0	NUM_LED	O
154	TXD/GPB1	CAP_LED	O
162	GPB2	SCRLL_LED	O
163	SMCLK0/GPB3	SMB0_CLK	IO
164	SMDAT0/GPB4	SMB0_DAT	IO
5	A20/GPB5	AZ0GATE	O
6	KBRST#/GPB6	RC_IN#	O
165	GPB7	THRO_CPU	O
47	CLKOUT/GPC0	/	
169	SMCLK1/GPC1	SMB1_CLK	IO
170	SMDAT1/GPC2	SMB1_DAT	IO
171	GPC3	/	
172	TMR10/WU2/GPC4	AC_IN_OC#	I
175	GPC5	OP_SD#	O
176	TMR11/WU3/GPC6	BAT1_IN_OC#	I
1	CK32KOUT/GPC7	/	
26	R11#WU0/GPD0	PM_SUSB#	I
29	R12#WU1/GPD1	PM_SUSC#	I
30	LPCRST#WU4/GPD2	BUF_PLT_RST#	I
31	ECSC#/GPD3	EXT_SC#	O
41	GPD4	RFON_SW#	I
42	GINT/GPD5	PM_SLP_M#	I
62	TACH0/GPD6	FANO_TACH	I
63	TACH1/GPD7	COLOREN#	I
87	ADC4/GPE0	/	
88	ADC5/GPE1	INTERNET#	I
89	ADC6/GPE2	MARATHON#	I
90	ADC7/GPE3	DISTP#	I
2	PWRSW/GPE4	PWR_SW#	I
44	WU15/GPE5	/	
24	LPCPD#WU16/GPE6	ME_ALERT#	I
25	CLKRUN#WU17/GPE7	PM_CLKRUN#	I
110	PS2CLK0/GPF0	/	
111	PS2DAT0/GPF1	/	
114	PS2CLK1/GPF2	/	IO
115	PS2DAT1/GPF3	/	IO
116	PS2CLK2/GPF4	TP_CLK	I
117	PS2DAT2/GPF5	TP_DAT	I
118	PS2CLK3/GPF6	/	
119	PS2DAT3/GPF7	INSTANT_ON#	I
113	FA16/GPG0	FA16	I
112	FA17/GPG1	FA17	I
104	FA18/GPG2	FA18	I
103	FA19/GPG3	FA19	I
3	FA20/GPG4	LID_SW#	I
4	PS2K0/GPF0	/	
5	PS2K1/GPF1	/	
6	PS2K2/GPF2	/	
7	PS2K3/GPF3	/	
8	PS2K4/GPF4	/	
9	PS2K5/GPF5	/	
10	PS2K6/GPF6	/	
11	PS2K7/GPF7	/	
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283	PS2K279/GPF279	/	
284	PS2K280/GPF280	/	
285	PS2K281/GPF281</		

- 1.H7415，H7417，H7419改?有潤濕點的type。
- 2.WLAN\_ON#(GPIO17) change to +3VS pull High
- 4.R5950,R5920 delte,重復上拉。Delete Q3901,Q3902
- 5.Delete the thermal sensor if GPU could get it's tempture by itself.
- 6.D6201 Spin power 改?在bead 后
- 8.SW7801 change to DIP at BOM
- 7.Delete D5102
- 9.82566 errata:add 10nf between +3V and 1.8vctrl and +1.0Vctrl
- 10.R2460,R2422,R2426 unstuff,R2323 pull Down
- 11.Add C2003,CN2201,CN2202,CN2206
- 12.SPI ROM P/N change to:05G001405010

<Variant Name>

		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	T11S	1.1	
Date: 2007.03.01		Sheet 3 of 95	

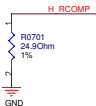






## RCOMP

For Calibrating the FSB IO Buffer



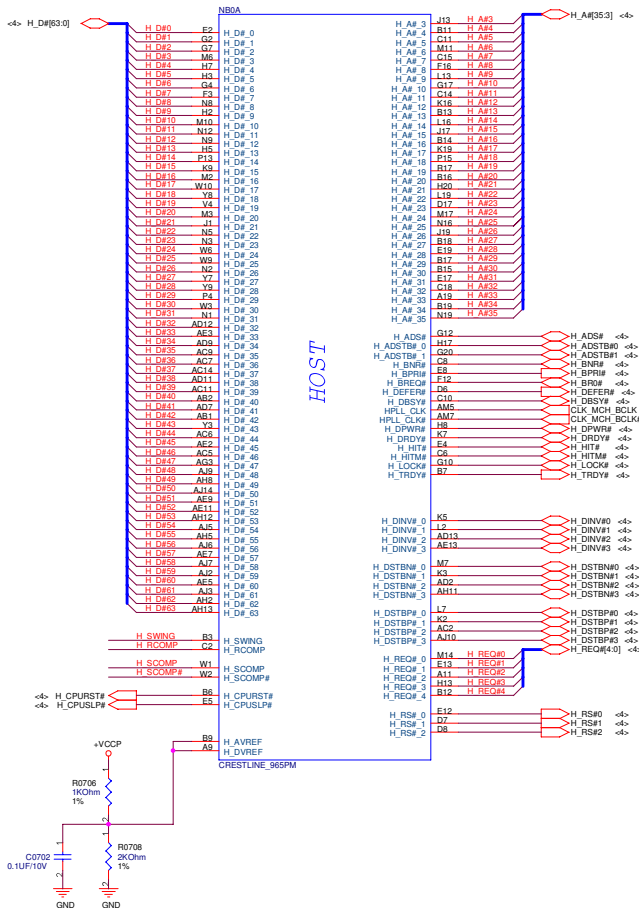
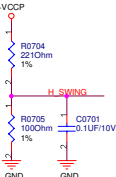
## SCOMP

For Slew Rate Compensation on the FSB

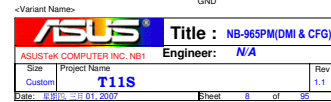


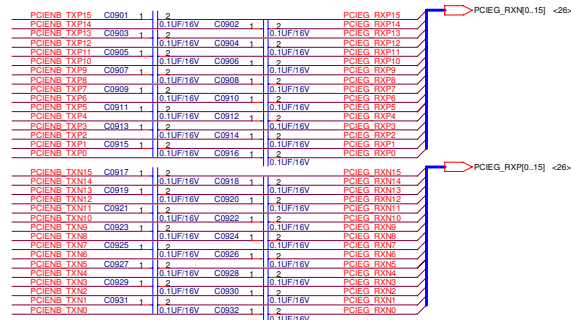
## Voltage Swing

For Providing a Reference Voltage to The FSB RCOMP circuits



<Variant Name>

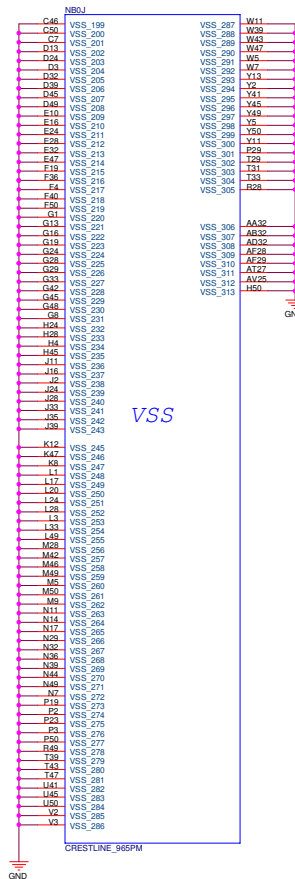
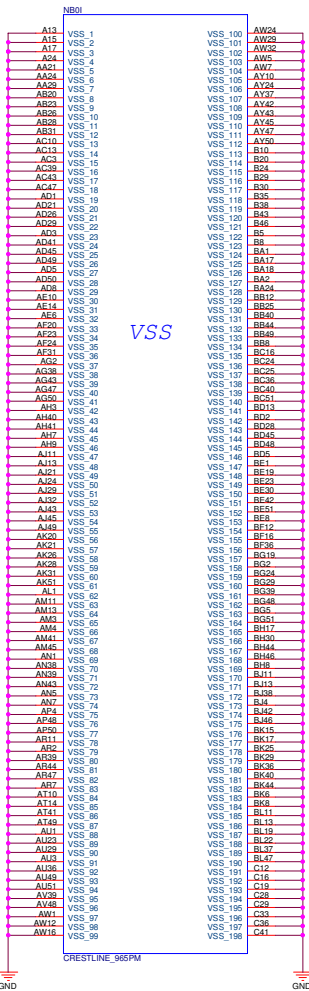






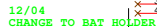






<Variant Name>





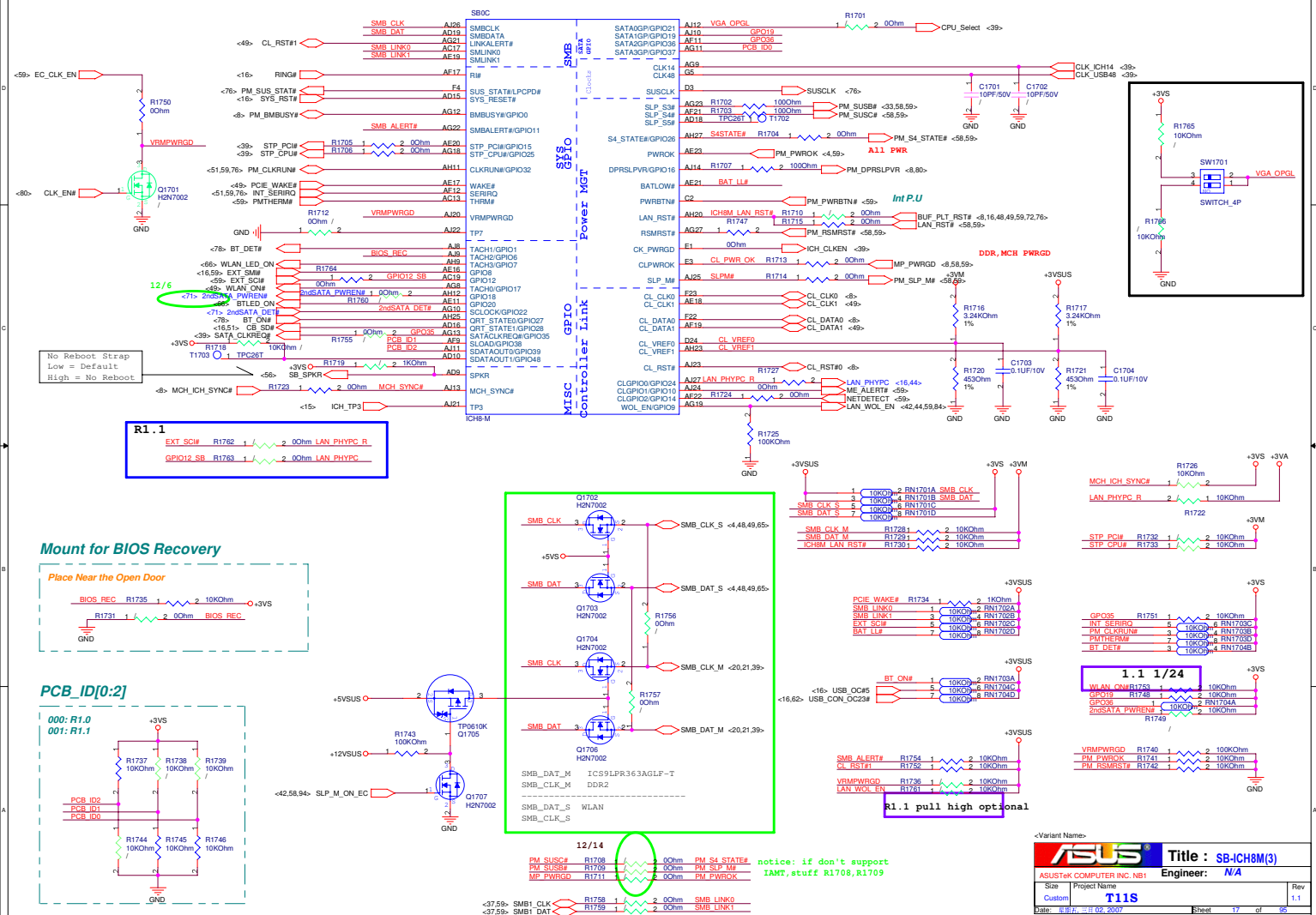
+VCC\_RTC

FOR 2nd HDD

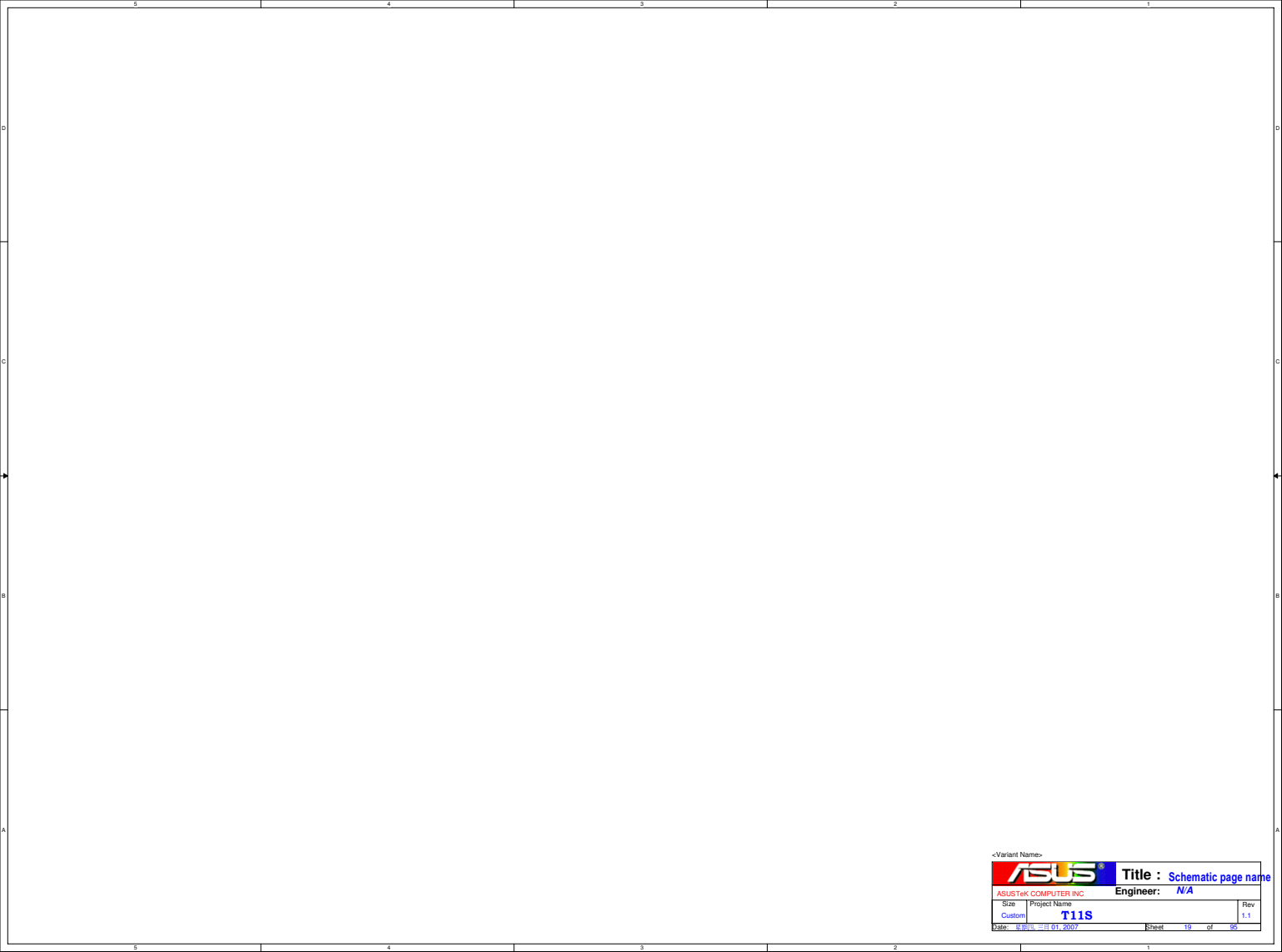
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<39> CLK_SATA_ICH#
<39> CLK_SATA_ICH
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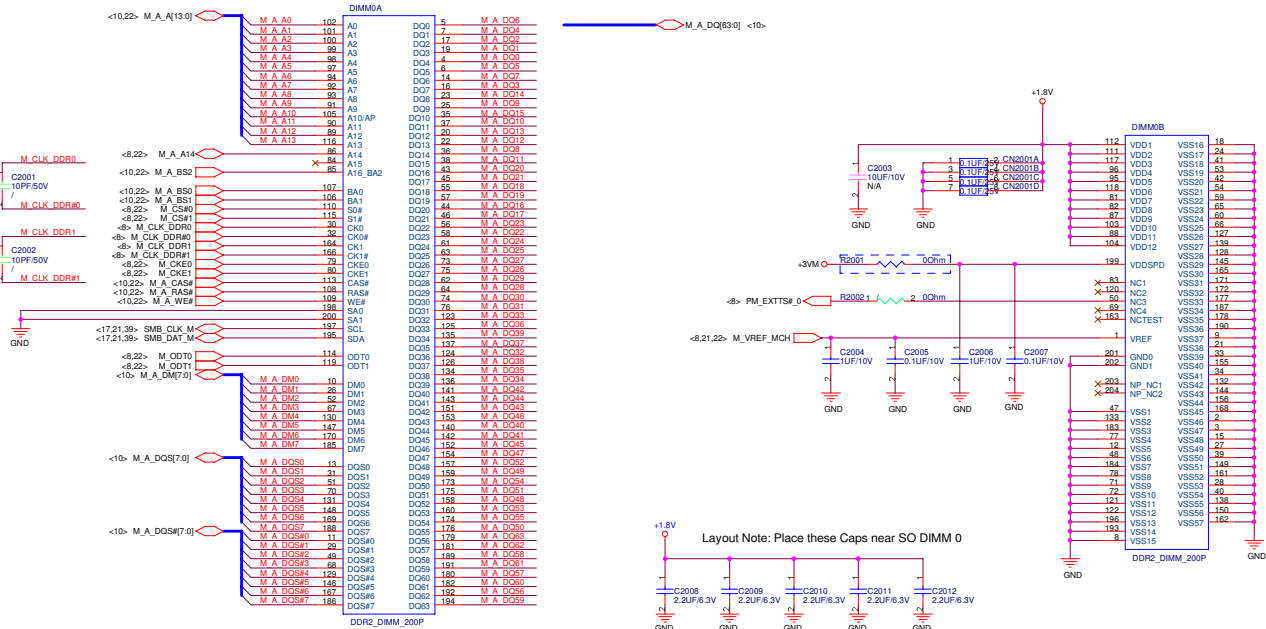








**REV Type**



Layout Note: Place these Caps near SO DIMM 0

<Variant Name>



**Title :** DDR2 SO-DIMM0

ASUSTeK COMPUTER INC. NB1

Engineer: N/A

Size

Project Name

	P <sub>0</sub>
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Size

Project Name **M11G**

114

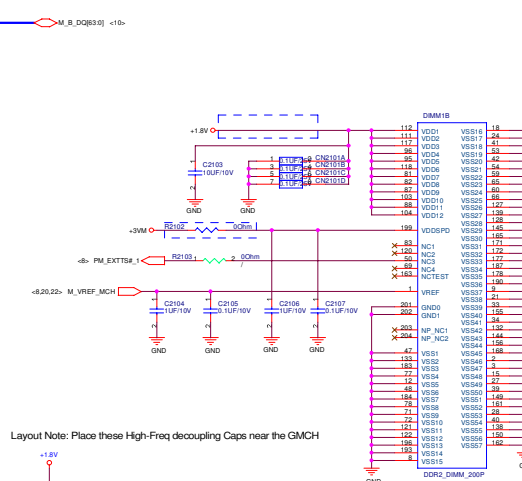
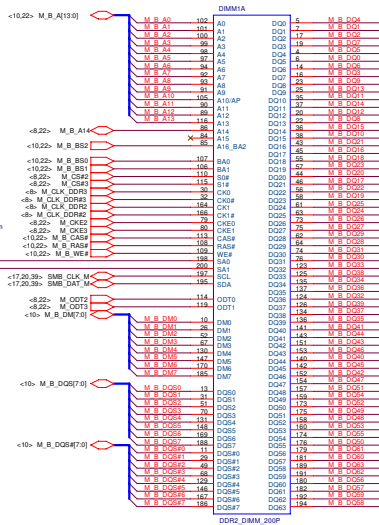
Custom

T11S

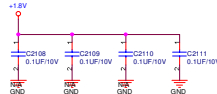
	1.1
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CHANGE THE P/N TO 12G025022004

### STD Type



Layout Note: Place these High-Freq decoupling Caps near the GMCH



**+1.8V**  
Layout Note: Place these Caps between SO DIMM 0&DIMM1



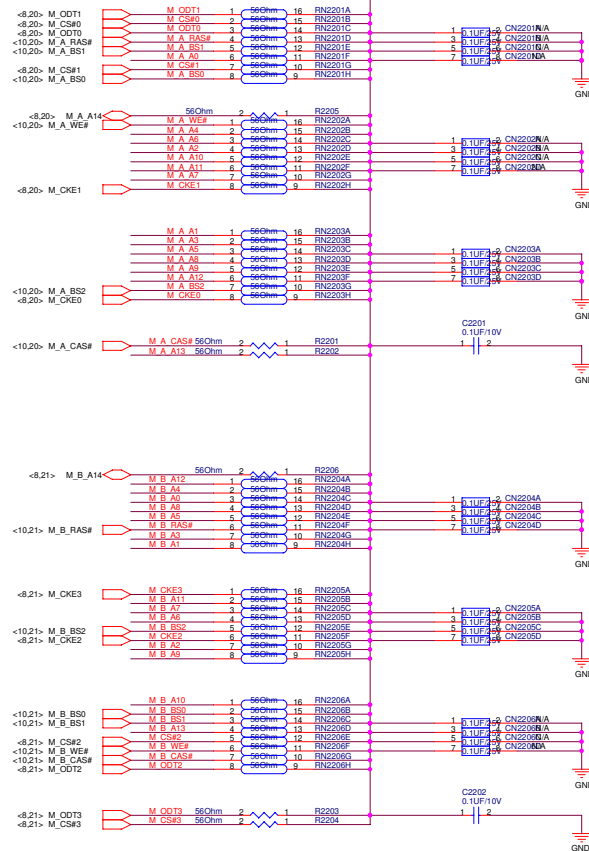
1.1 1/24 add CAP

<Variant Name>



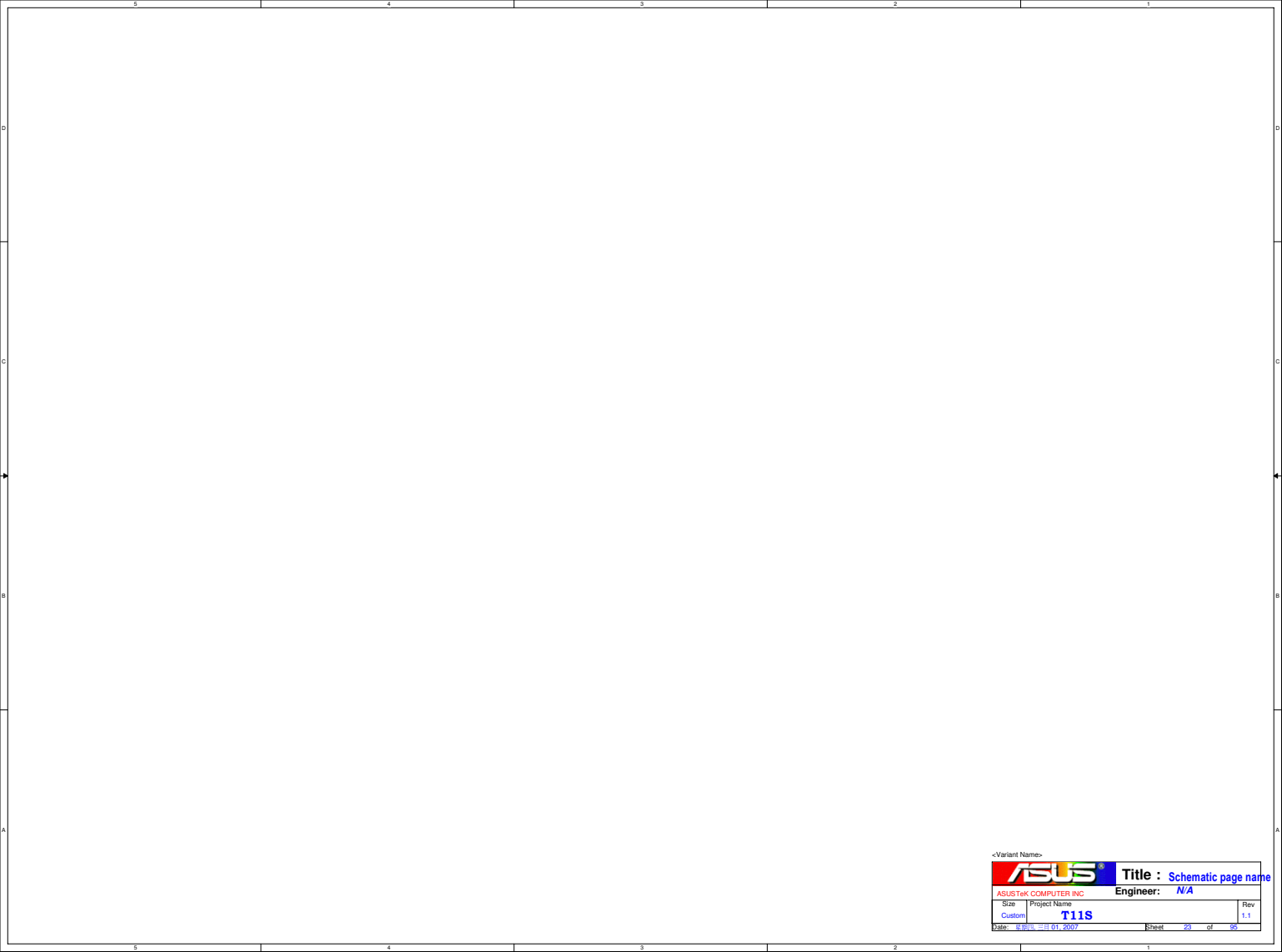
12/4 Delete PJP2201

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<10.21> M\_B\_A[13:0]

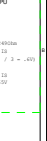
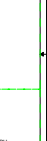
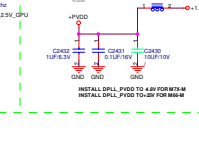
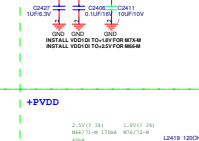
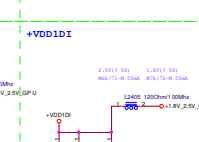
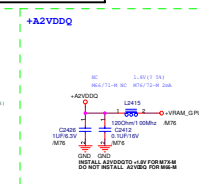
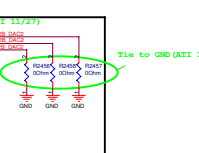
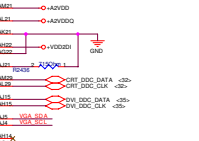
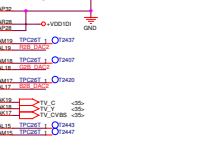
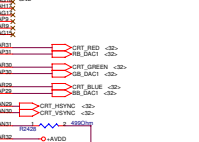
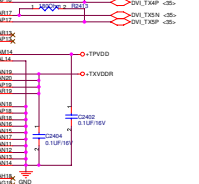
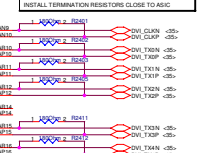
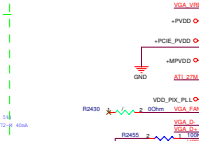
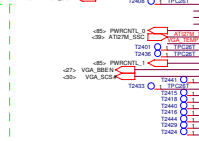
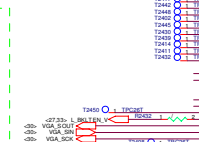
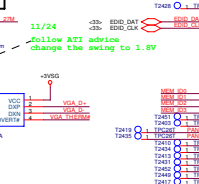


<Variant Name>

<b>ASUS</b>		<b>Title : DDR2 TERMINATION</b>	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 8/30/2007 10:01:00	Sheet	22	of 95



---SRS : 0 / 1 / NC.



\* xxxM Mem

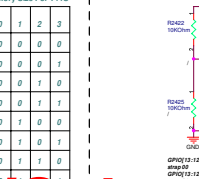
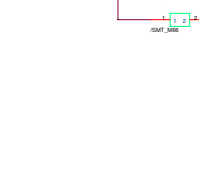
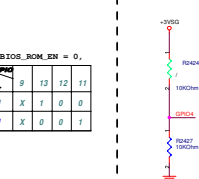


Figure 10 shows the schematic diagram of the input stage of the proposed 100-GHz CMOS divider. The input stage consists of a differential pair of NMOS transistors (M1, M2) with a tail current source (M3). The gates of M1 and M2 are driven by a differential-mode input signal ( $V_{in,dm}$ ). The drains are connected to a differential-mode load consisting of two 10kΩ resistors (R2422, R2425) in series with a 10kΩ resistor (R2426) connected to ground. The output signals are taken from the drains of M1 and M2.

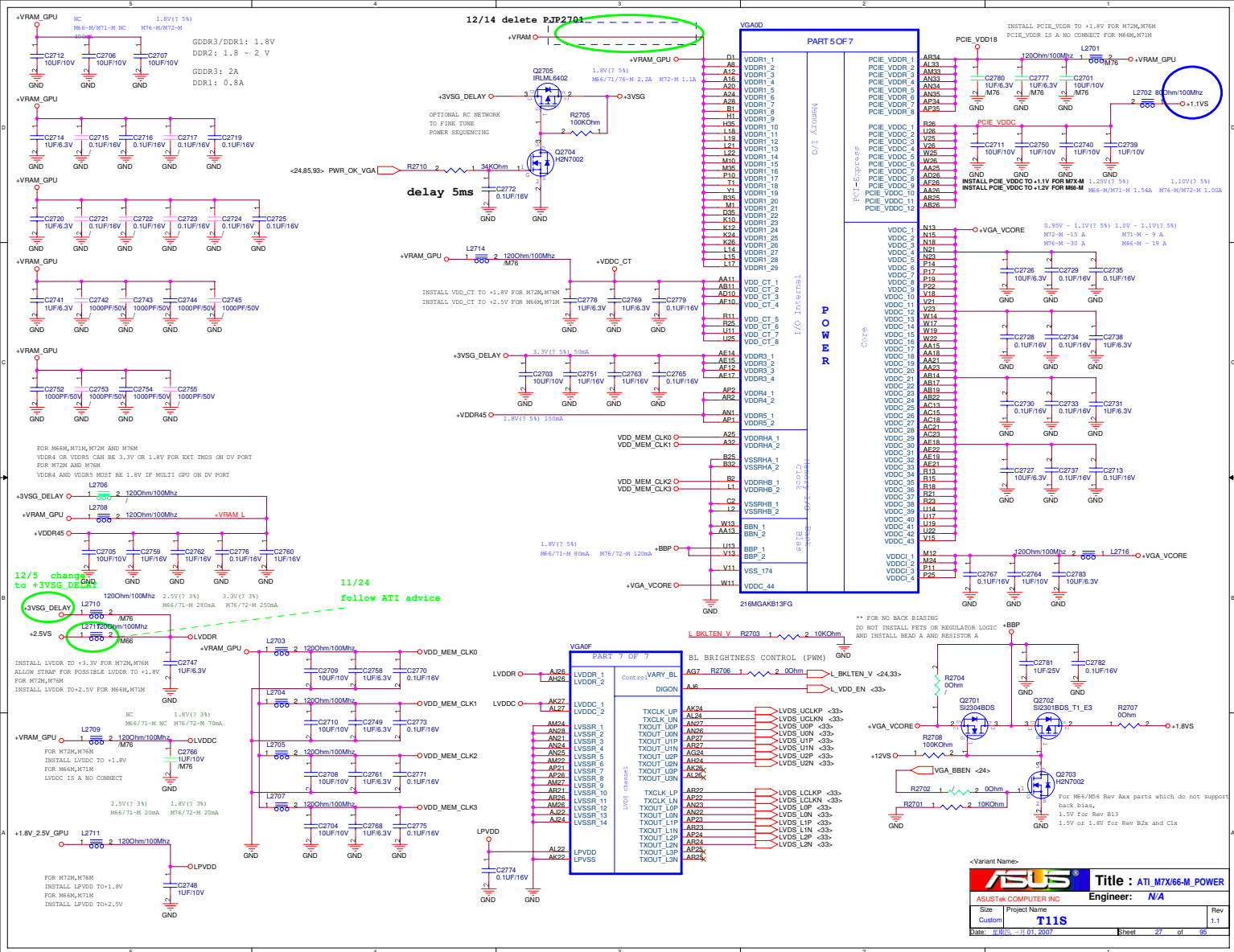


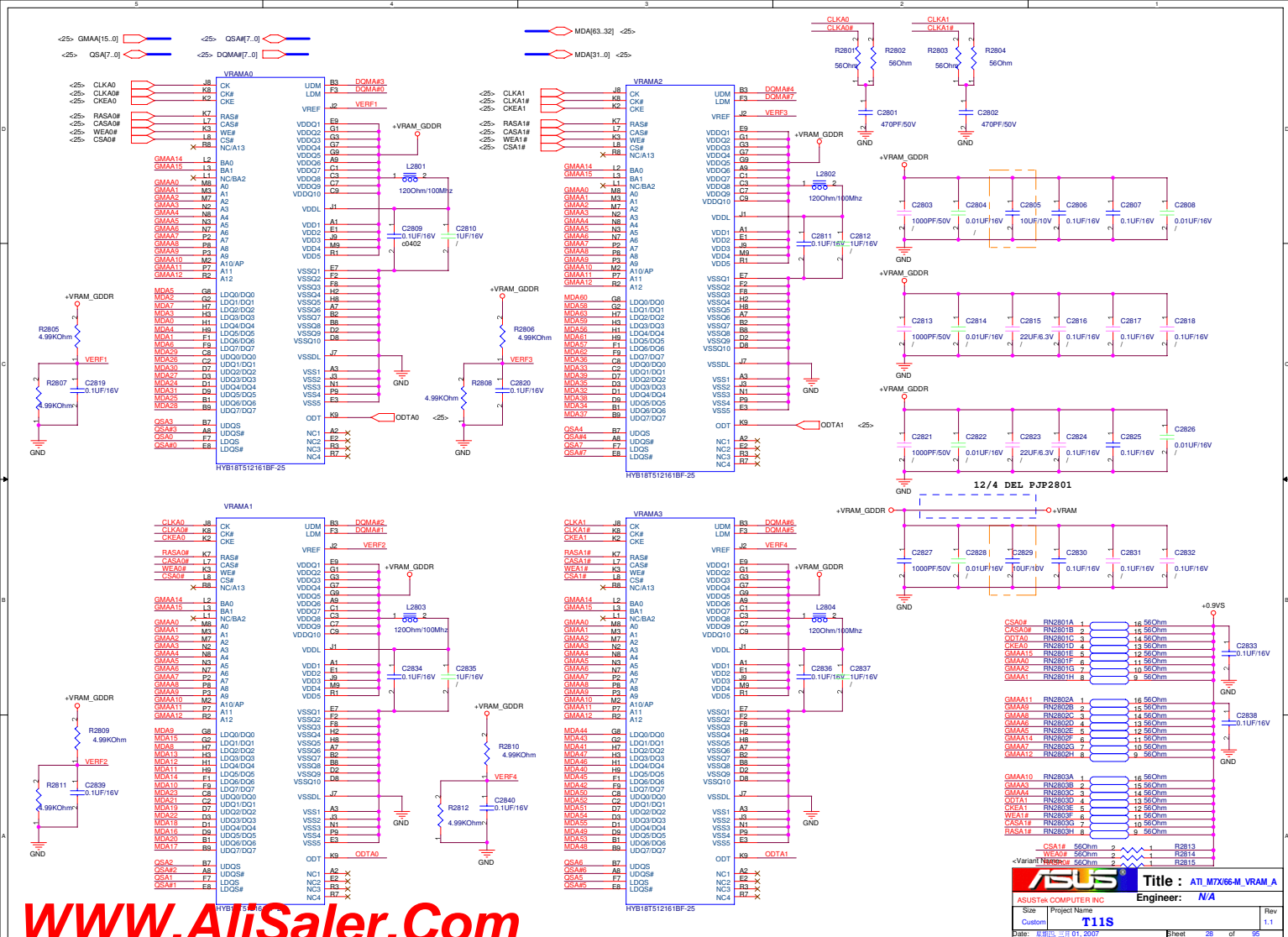
\_\_\_\_\_

M\_MAIN

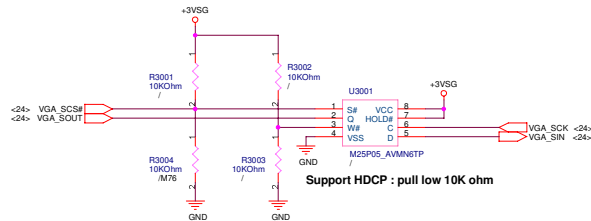
		<b>Title :</b> ATI_M7X/66-M_Memory	
<b>ASUSTek COMPUTER INC</b>		<b>Engineer:</b> N/A	
Size Custom	Project Name T11S	Rev 1.1	
Date: 2007年3月1日		Sheet 25	of 95







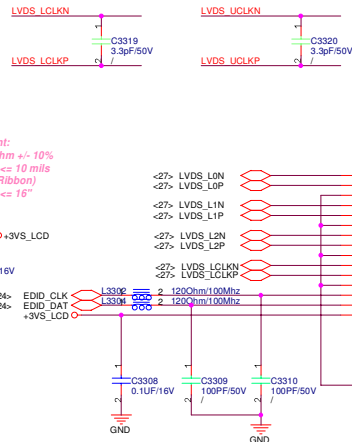




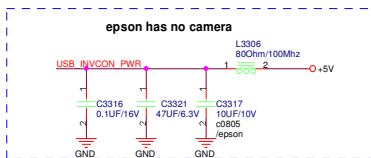
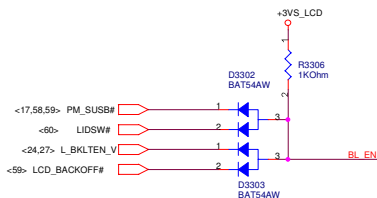
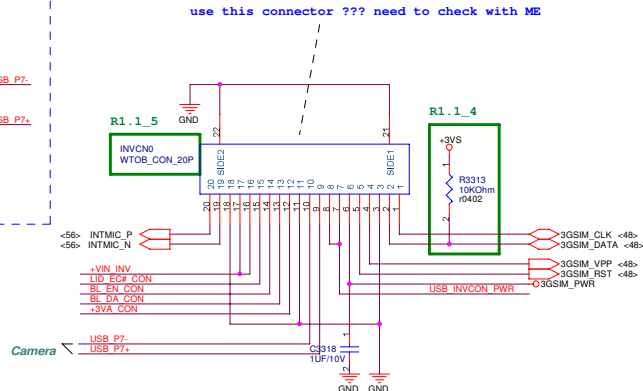
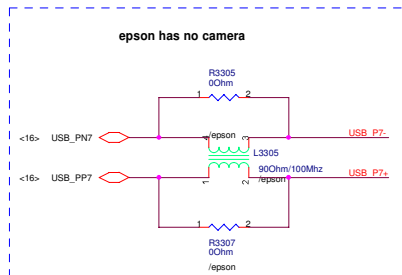
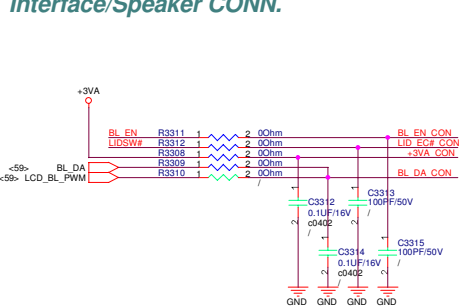




## LCD Power



**INVERTER**  
**Interface/Speaker CONN.**



&lt;Variant Name:



**Title :** I VDS & INVERTED

ASUSTeK COMPUTER INC.

Engineer: **N/A**

Size	Project Name
------	--------------

T11

1

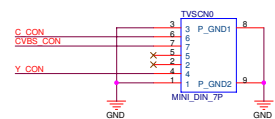
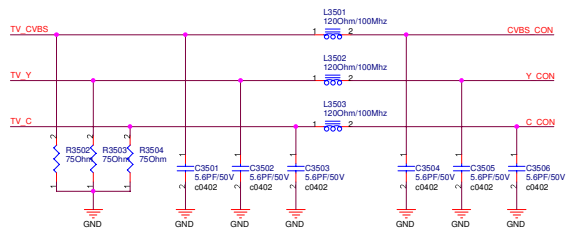
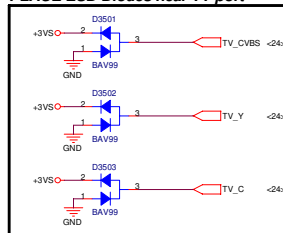
Date: 04/09/07 11:01 01 2007

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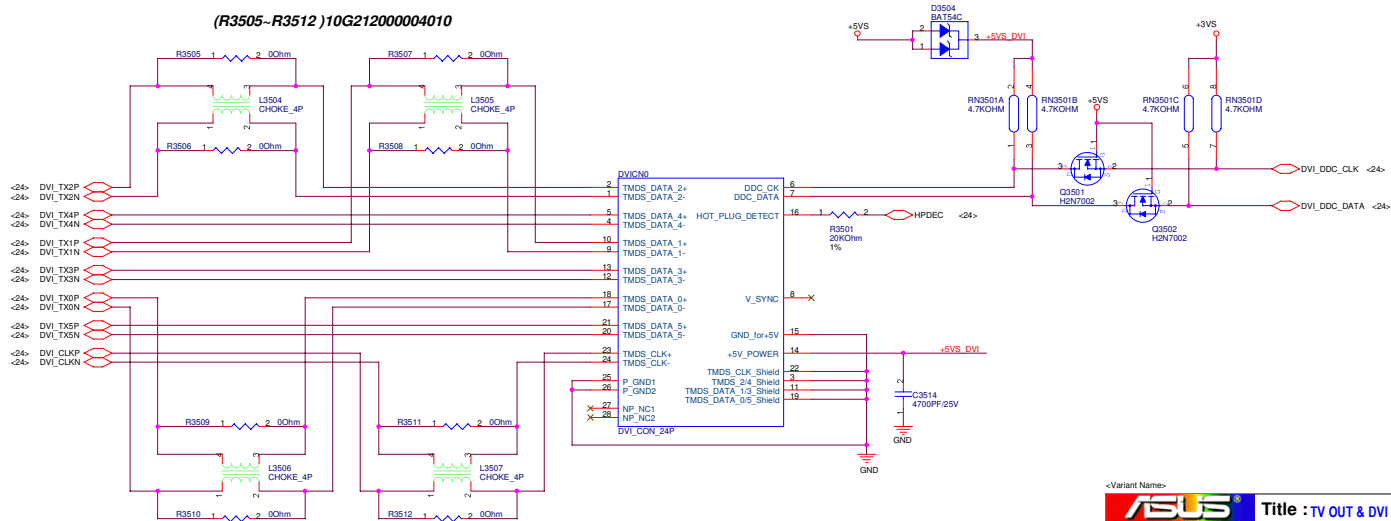
# TV OUT

## PLACE ESD Diodes near TV port



# DVI

## (R3505-R3512) 10G212000004010

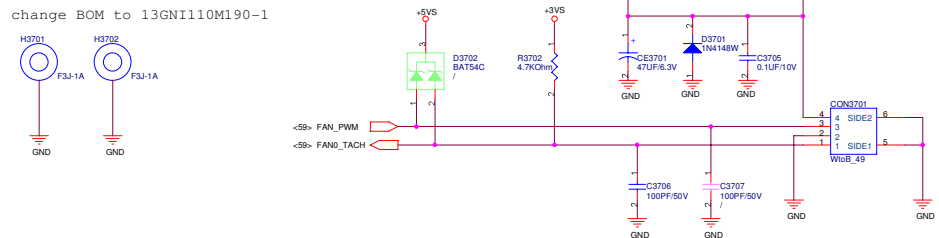


<Variant Name>

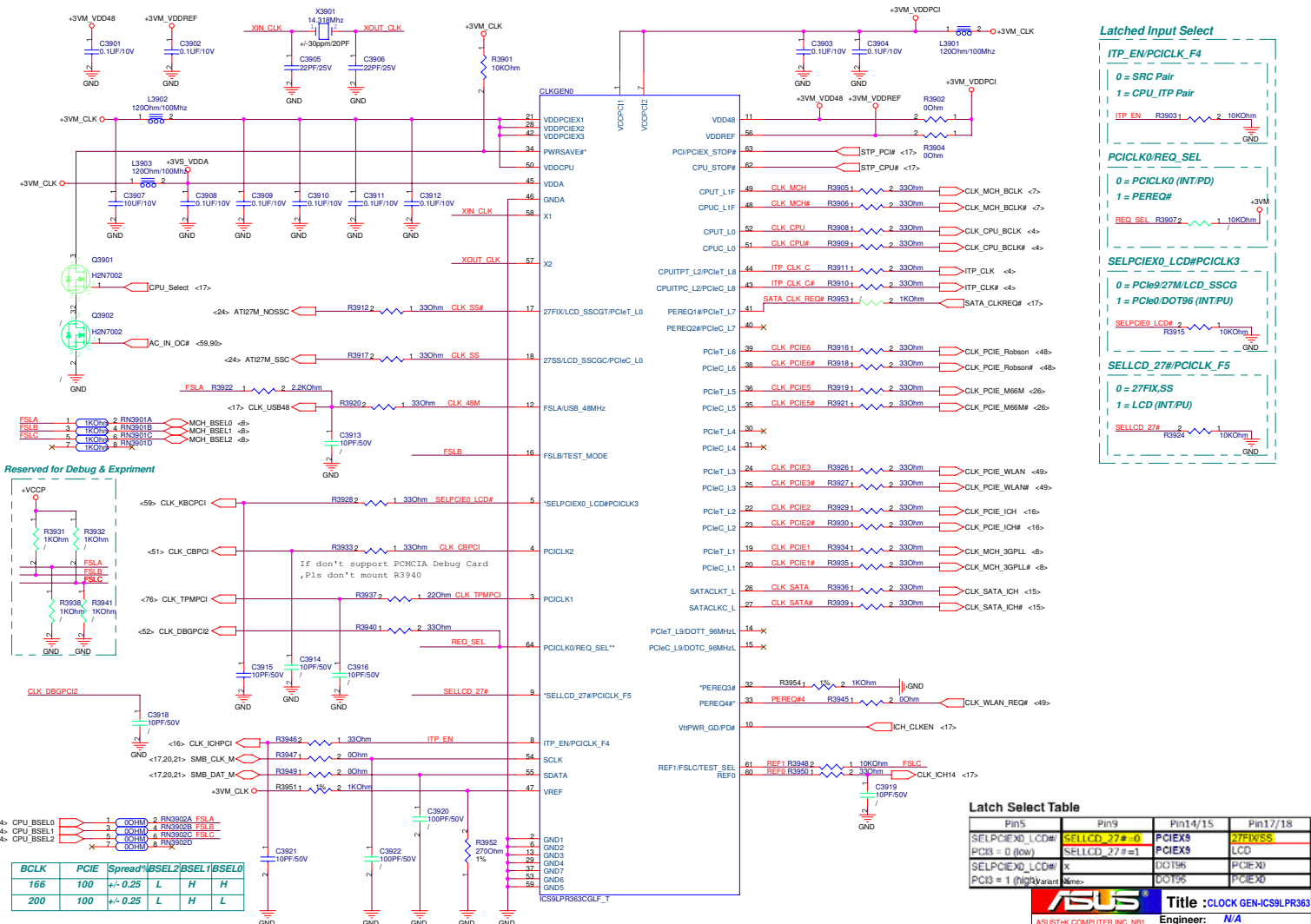
<b>ASUS</b>		<b>Title : TV OUT &amp; DVI CON.</b>	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	<b>T11S</b>		1.1
Date: 01/01/2007		Sheet	35 of 95



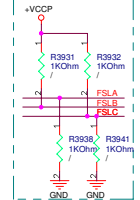
## DC FAN Control







Reserved for Debug & Experiment



BCLK	PCIE	Spread#	BSEL2#	BSEL1#	BSEL0
166	100	+/- 0.25	L	H	H
200	100	+/- 0.25	L	H	L

Latched Input Select

ITP\_EN/PCICLK\_F4

0 = SRC Pair  
1 = CPU\_ITP Pair

PCICLK0/REQ\_SEL

0 = PCICLK0 (INT/PD)  
1 = PEREQ#

SELPCIE\_X0\_LCD#/PCICLK3

0 = PCIe9/27M/LCD\_SSCG  
1 = PCIe0/DOT96 (INT/PU)

SELLCD\_27#/PCICLK\_F5

0 = 27FX/SS  
1 = LCD (INT/PU)

Latch Select Table

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE_X0_LCD#	PCICLK_27# = 0	PCIE_X9	27FX/SS
PCIS = 0 (low)	SELLCD_27# = 1	PCIE_X9	LCD
SELPCIE_X0_LCD#	X	DOT96	PCIE_X0
PCIS = 1 (high/standby)	X	DOT96	PCIE_X0

ASUS®

ASUSTeK COMPUTER INC. NBI

Engineer: N/A

Size: Project Name: T11S


Date: 2007.01.01

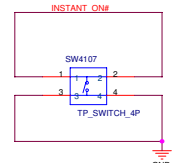
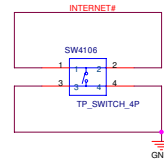
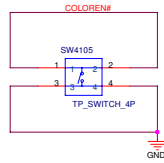
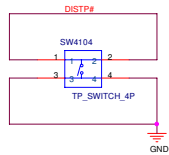
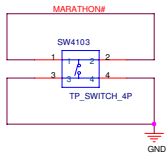
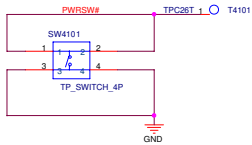
Sheet: 39 of 45

Rev: 1.1

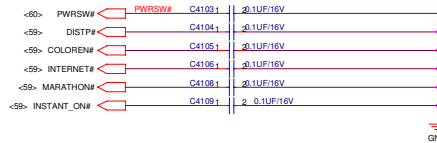
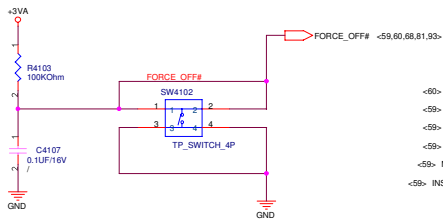
R1.1 change to 270 ohm to adjust the clk cross point

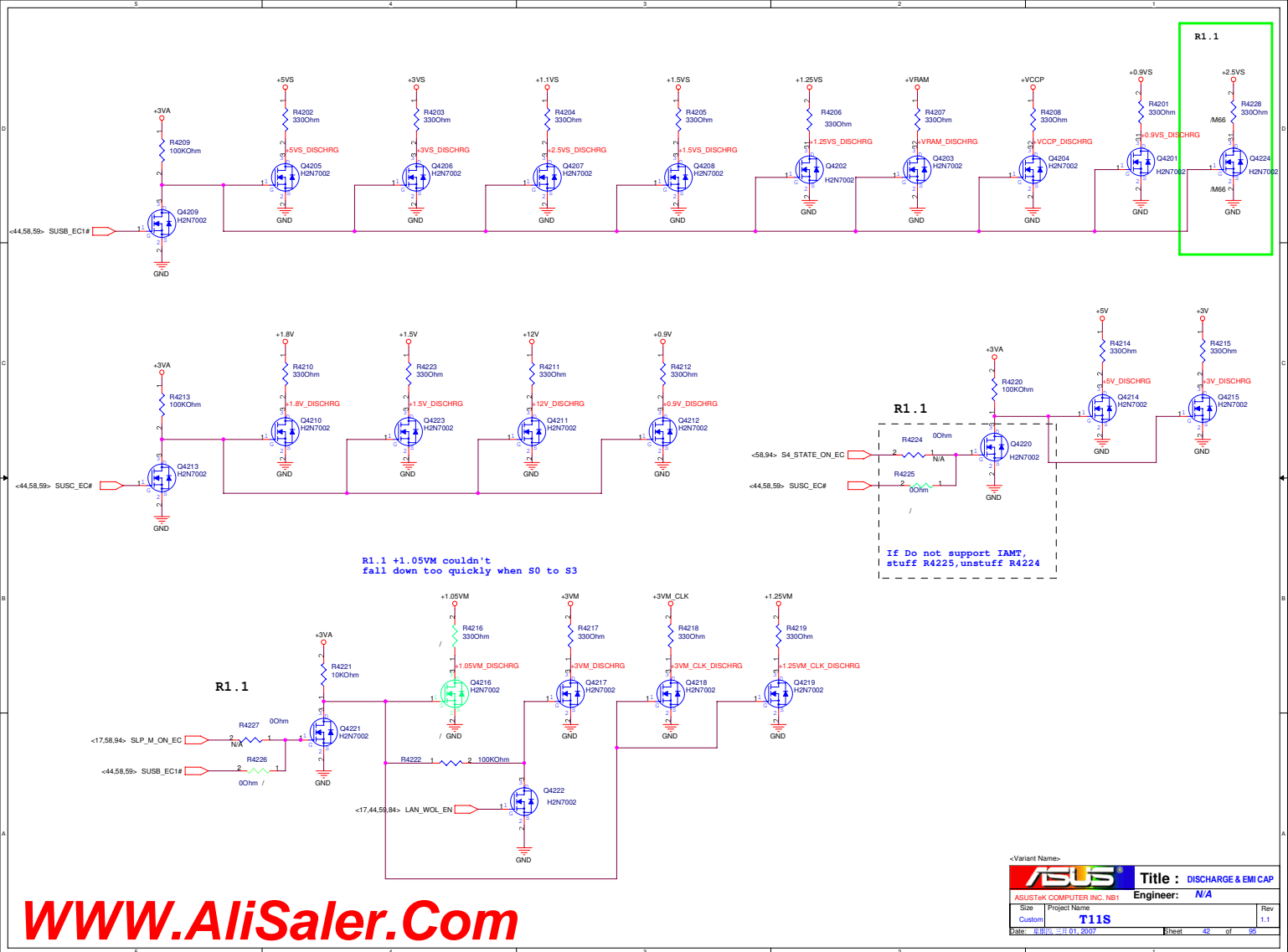
<Variant Name>

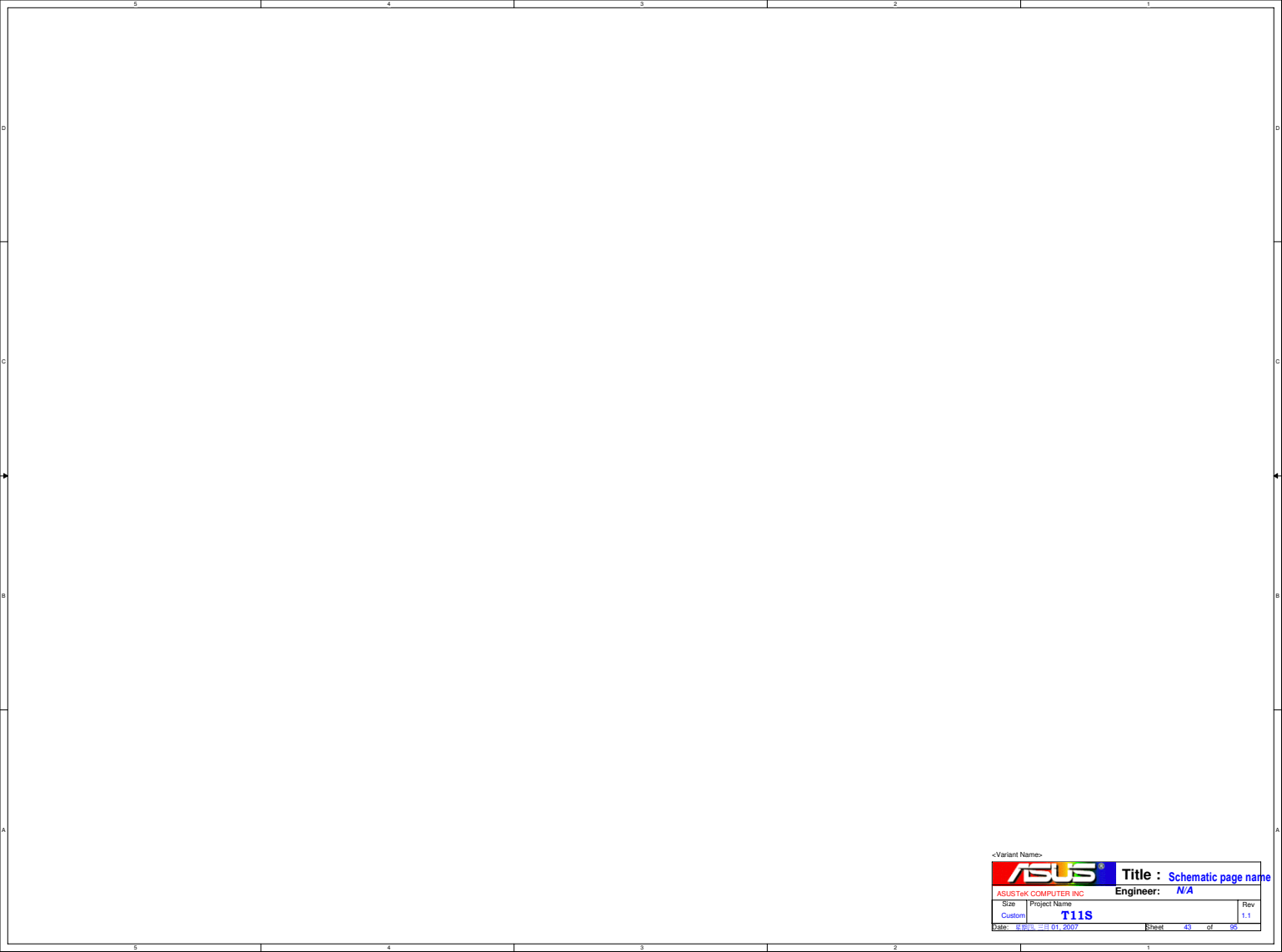
		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 01/01/2007		Sheet 40 of 95	



## SHUT\_DOWN#

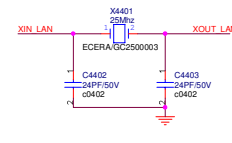






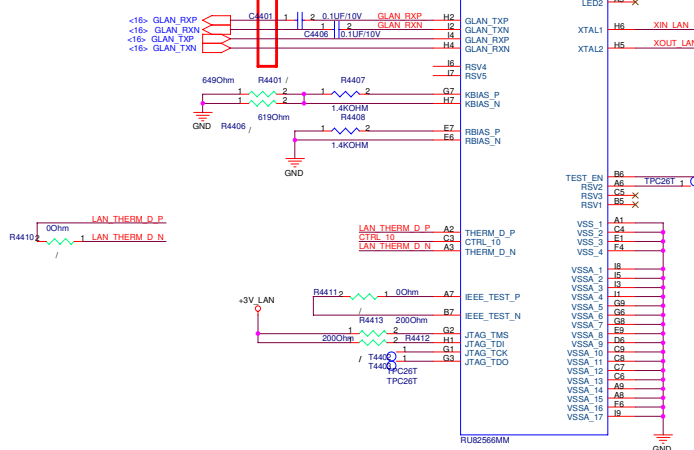
Differential 95 ohm(top/bot) 100 ohm (in1/in2/in3) +/-20%  
0.5"total length+4" Space+12mil Max via:6 breakout <0.25" +/-50 mil length match

## Crystal

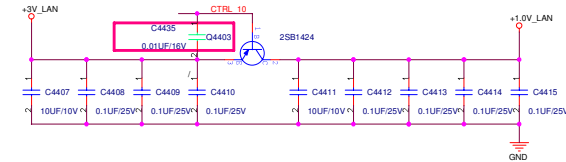


layout: 55 ohm +/-15% length<14"  
LAN\_TXD[0:2], LAN\_RXD[0:2] must be equal(5500mil)

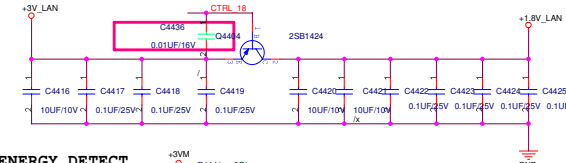
Differential 95 ohm(top/bot)  
100 ohm (in1/in2/in3) +/-20%  
Total length<17" Max via:6



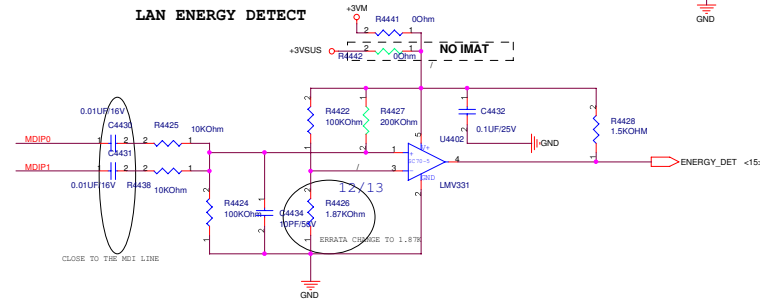
1.1 1/24 add CAP  
intel errata



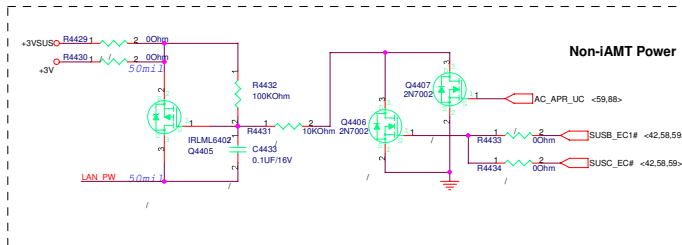
1.1 1/24 add CAP  
intel errata



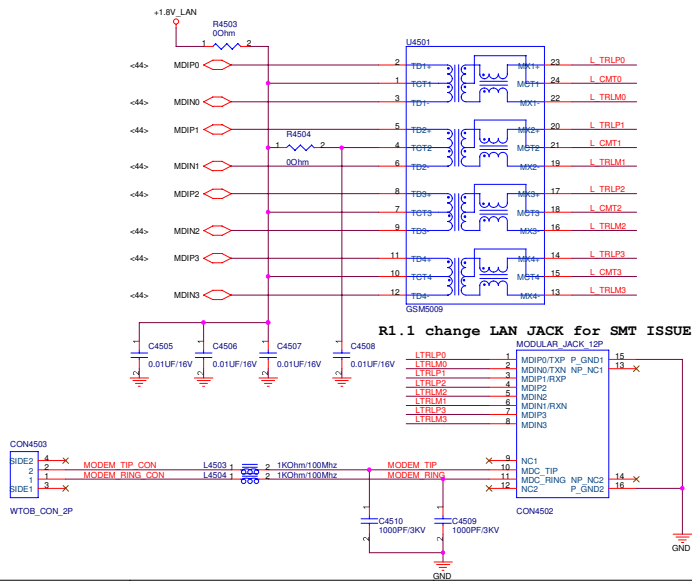
## LAN ENERGY DETECT



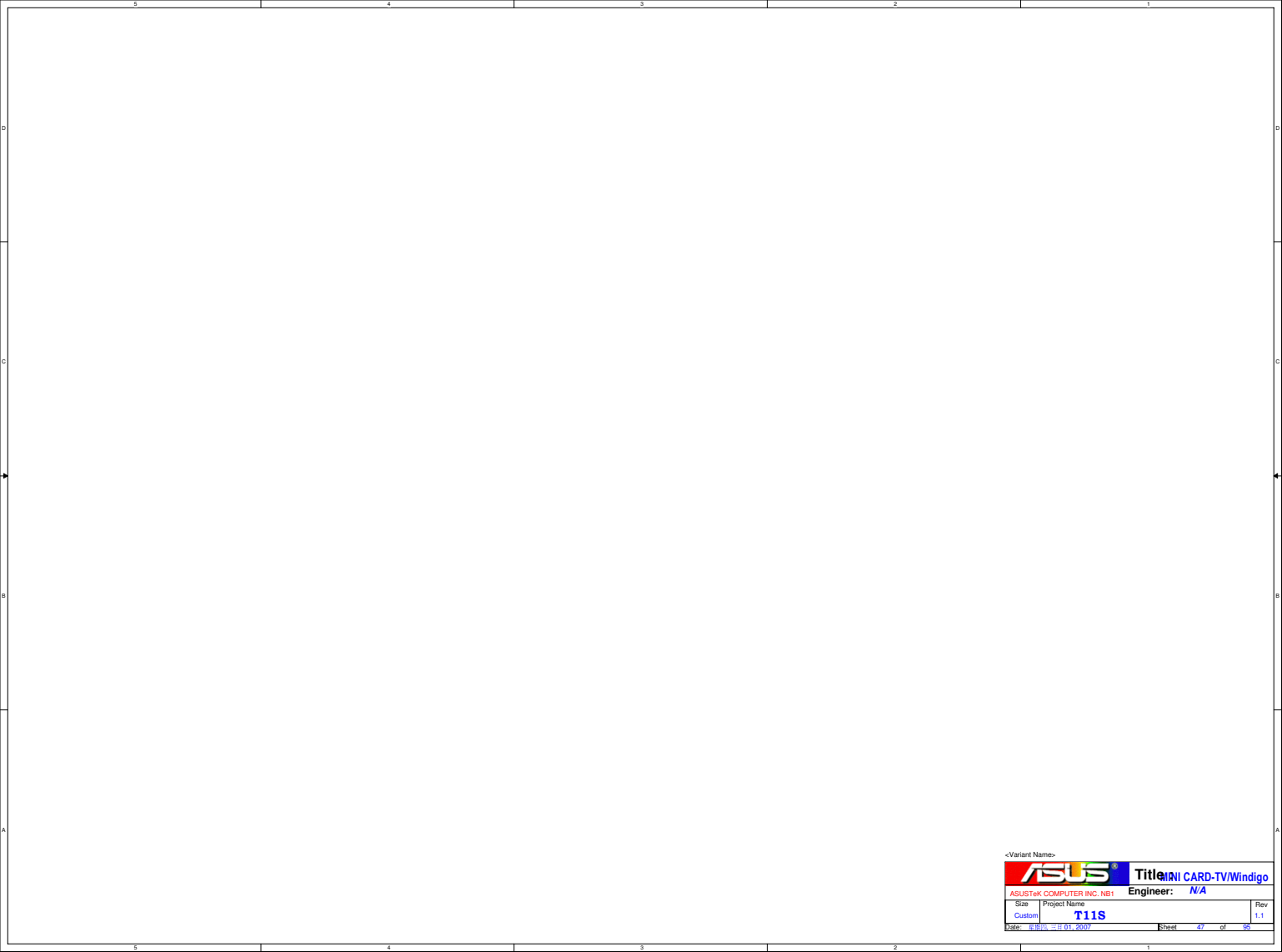
## Non-iAMT Power



## LAN CONN.







<Variant Name>

		Title: NI CARD-TV/Windigo	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 01/01/2007		Sheet	47 of 95

# Robson Windigo

Windigo  
stuff these

Robson

Robson

Robson

Windigo  
+3.003V~+3.597V  
Max= 2750 mA  
Max=3.1W

Robson  
+1.425V~+1.575V  
Max= 400 mA

Windigo  
stuff these

Windigo

The top side depends on CD-ROM connect to put the board

<48> WLANmC2\_REQ# R4803 1 2 00hm mC2\_REQ#

stuff these

Windigo

change to 13G021043011



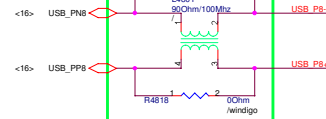
H4801  
A40M20-6AAS



H4802  
A40M20-6AAS

Windigo

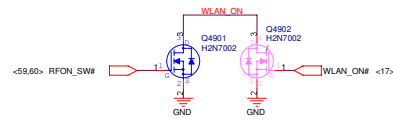
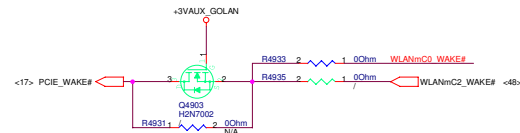
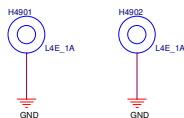
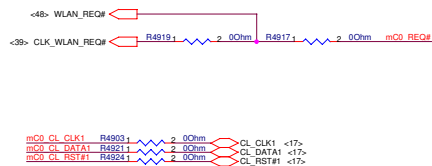
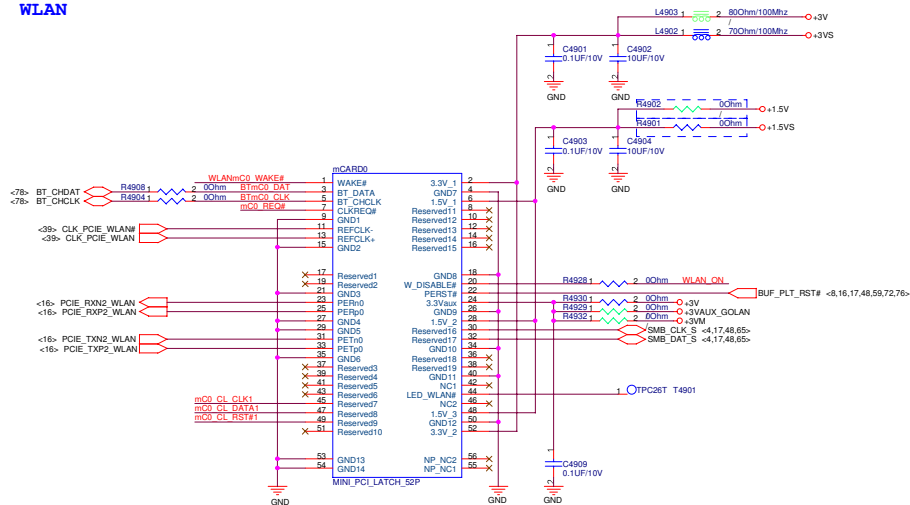
stuff these



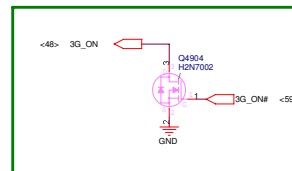
<Variant Name>

ASUS		Title : MINI CARD-Robson	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 09/06/2007		Sheet 48 of 95	

# 1. Kedron WLAN



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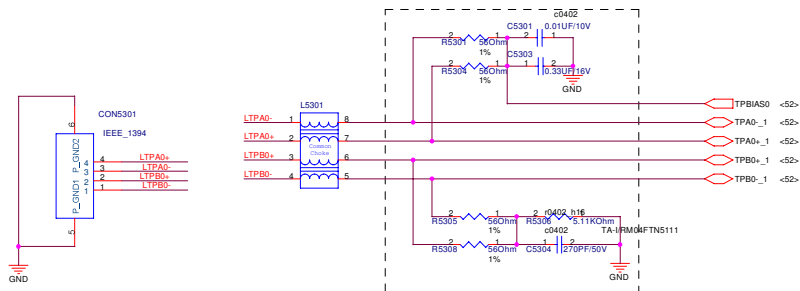
<Variant Name>

<Variant Name>

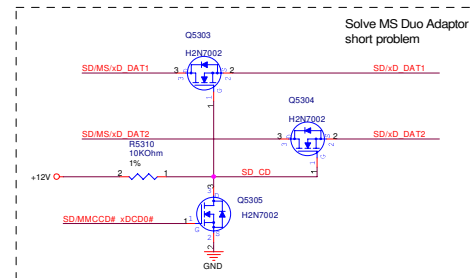
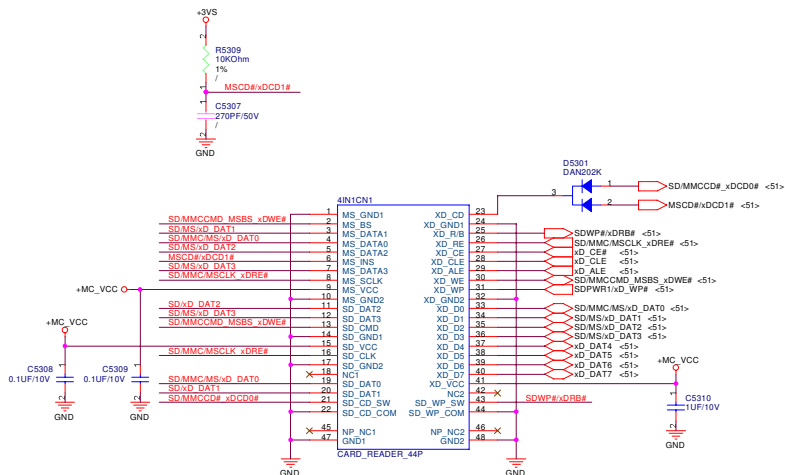
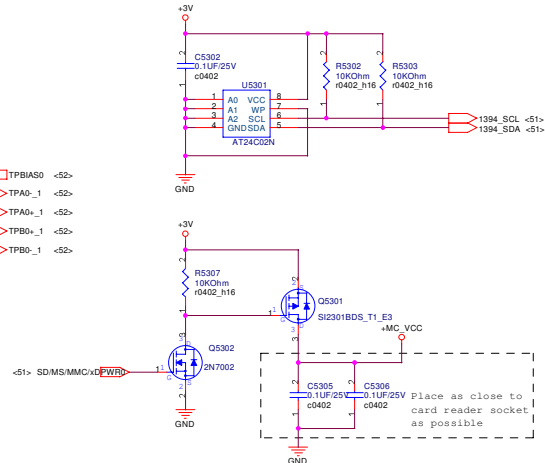
		Title : Schematic page name	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 01/01/2007		Sheet	50 of 95





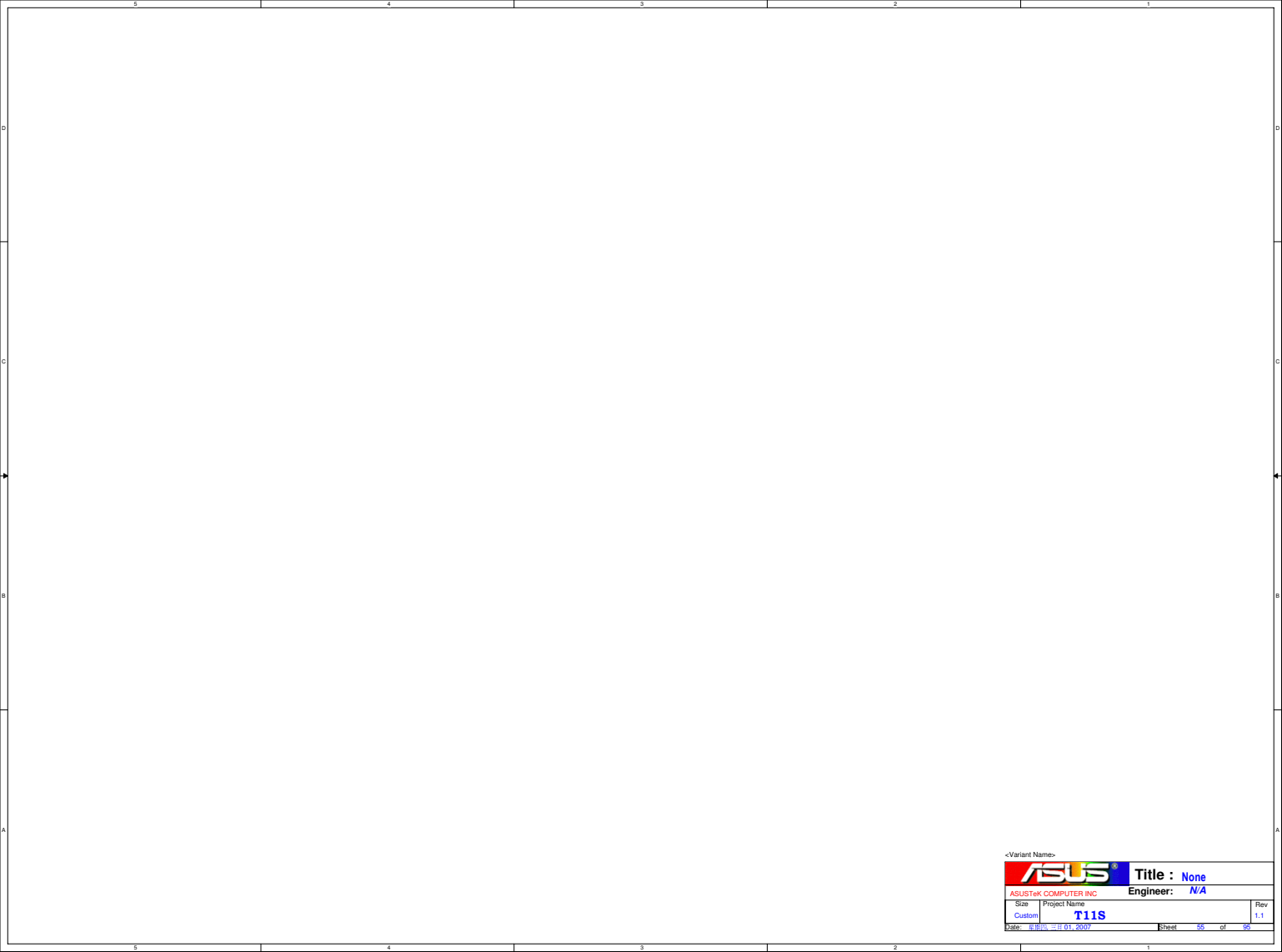


1. CLOSE TO R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend , maxmium is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm




<Variant Name>

		Title : NEWCARD	
ASUSTeK COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
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<Variant Name>



Title : **None**

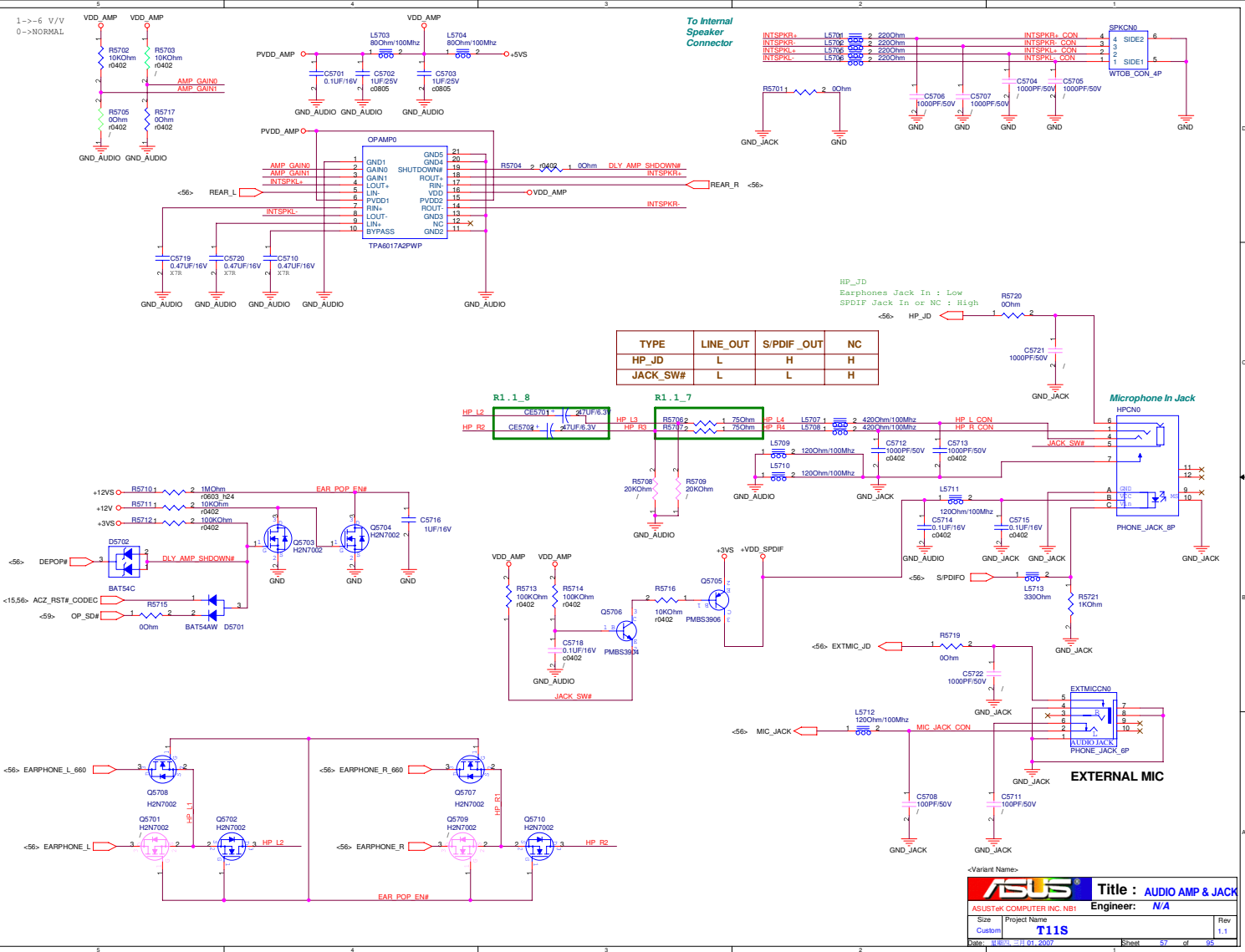
ASUSTeK COMPUTER INC

Engineer: **N/A**

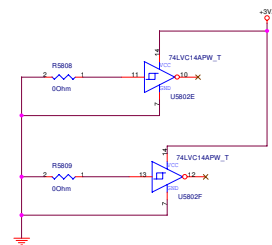
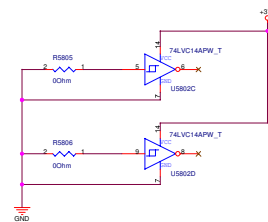
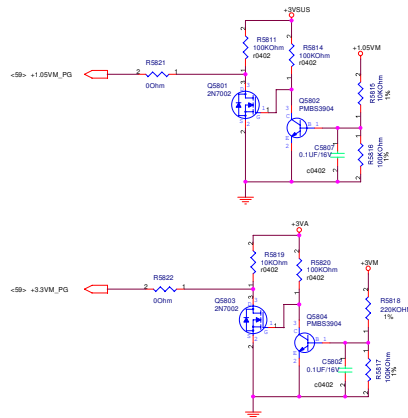
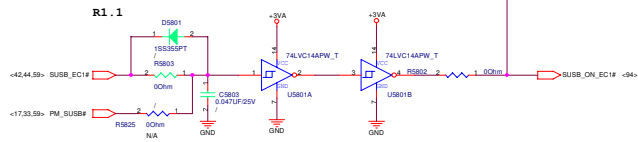
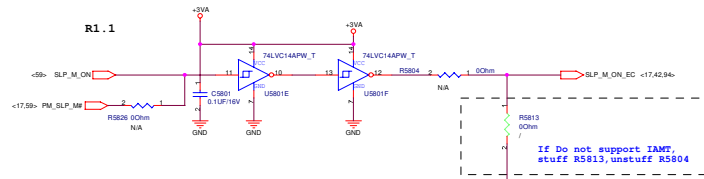
Size	Project Name	Rev
Custom	<b>T11S</b>	1.1
Date: 6/26/2007		Sheet 55 of 95



```
1->-6 V/V
0->NORMAL
```

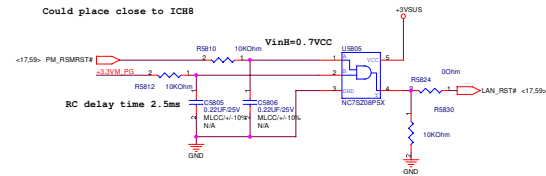


R1.1 for support AMT sequence, modify the sequence by H/W



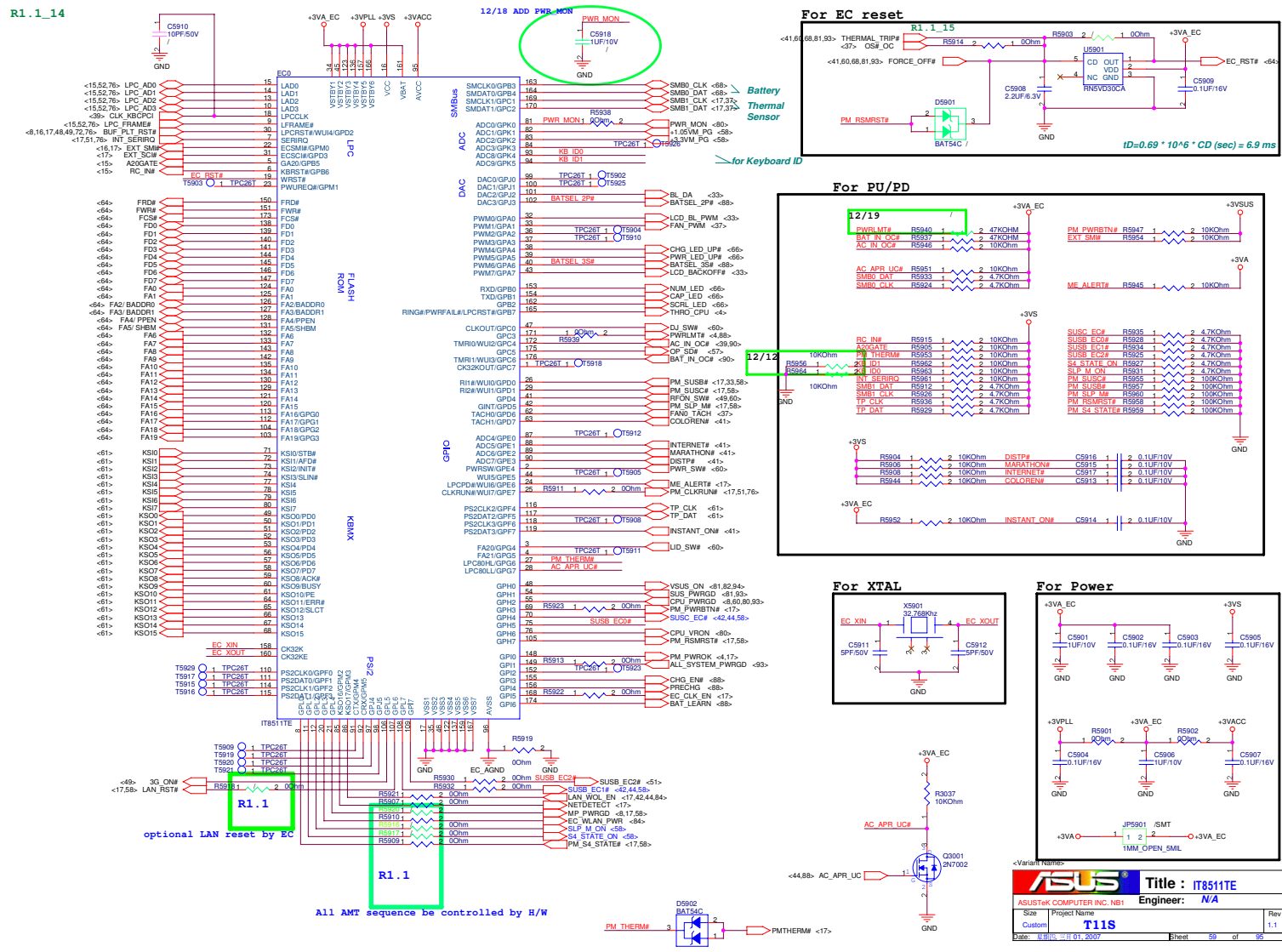
**R1.1**

Could place close to ICBS



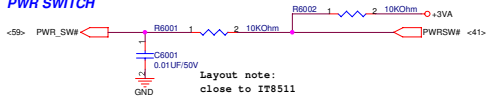
<Variant Name>

R1.1\_14

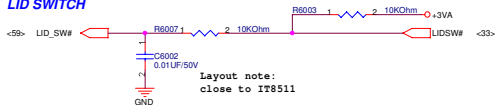


## For Switch

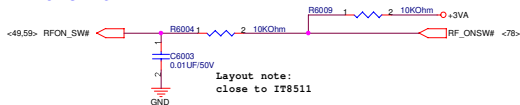
## PWR SWITCH



## LID SWITCH

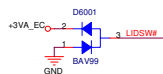


## RF ON SWITCH



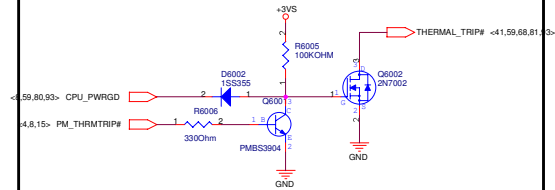
## Note:

This LID\_EC# is a signal from inverter board, it is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. It needed to add bidirectional diode to protect this pin.



Layout note:  
close to connector

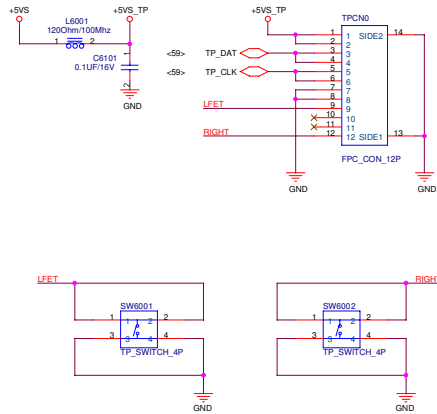
## For Thermal Control Method



&lt;Variant Name&gt;

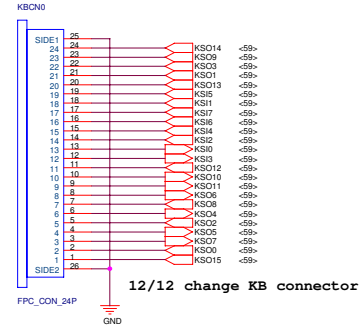
<b>ASUS</b>		Title : Schematic page name	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 2007/03/01	Sheet 60 of 95		

*For Touch-Pad*

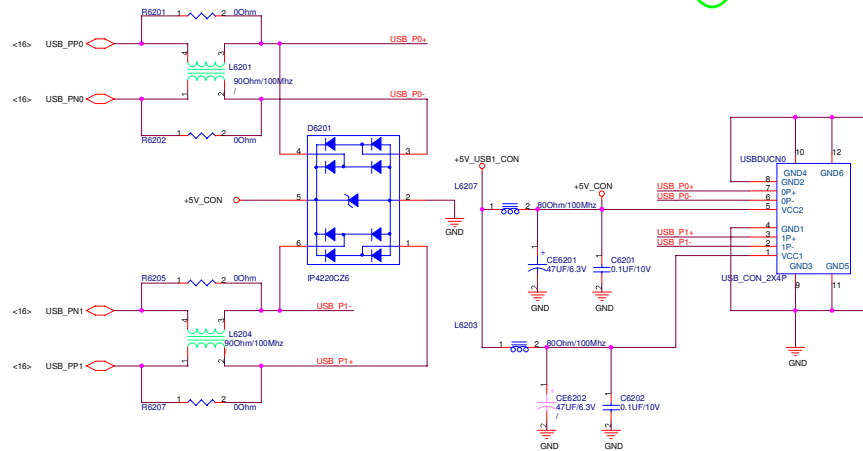


*For Keyboard*

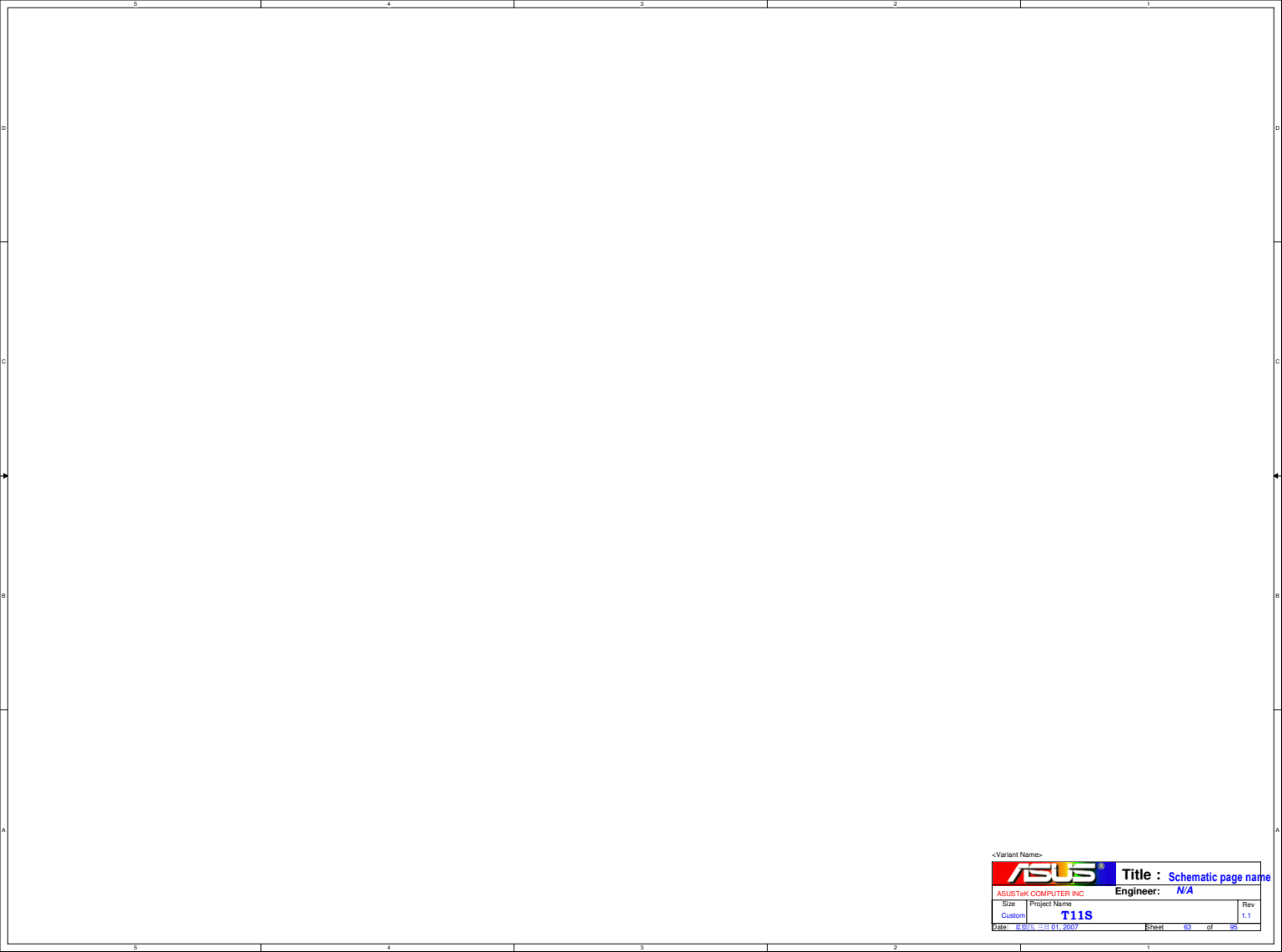
R1.1 modify the pin connect



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		<b>Title : USB CONN</b>	
<b>ASUSTeK COMPUTER INC</b>		<b>Engineer: N/A</b>	
Size Custom	Project Name <b>T11s</b>	Rev 1.1	
Date: 壹零玖年三月一日, 2007		Sheet 62	of 95



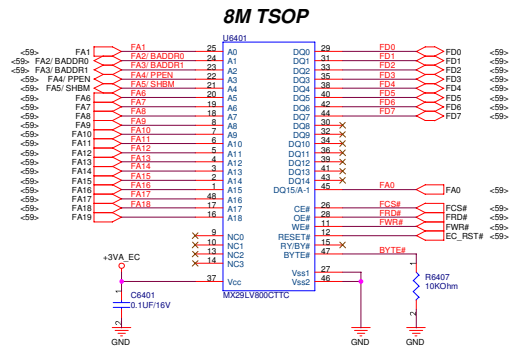
**FA2/ BADDR0 & FA3/ BADDR1**

00: PNPCNG Access Register Pair are 002Eh and 002Fh  
 10: PNPCNG Access Register Pair are 004Eh and 004Fh  
 01: PNPCNG Access Register Pair are Determined by  
 EC Domain Registers SWCBALR and SWCBAHR.  
 11: Reserved

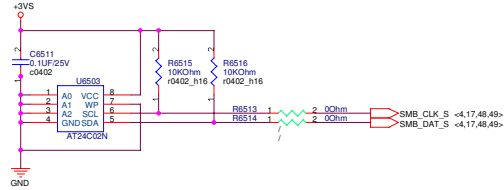
**FA4/ PPEN**

0: Normal  
 1: KBS Interface Pins are Switched to Parallel Port  
 Interface for In-System Programming

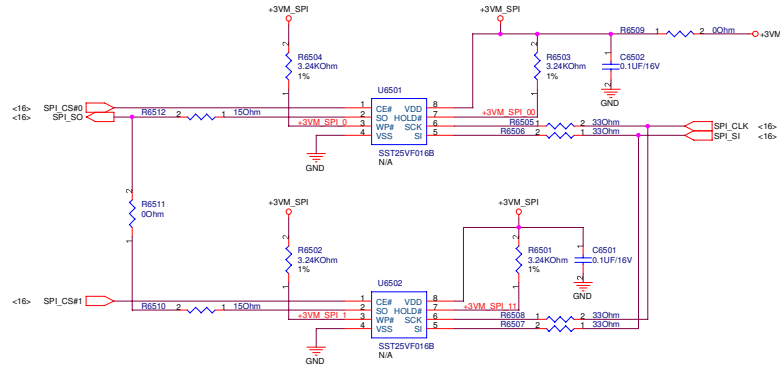
*Note: Sampled at VYSTBY Power Up Reset*



# DETECT Open GL/or None Open GL

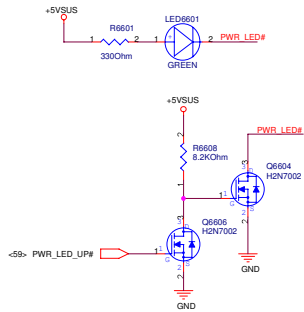


## 1.1 1/24 change to 16Mbit SPI flash

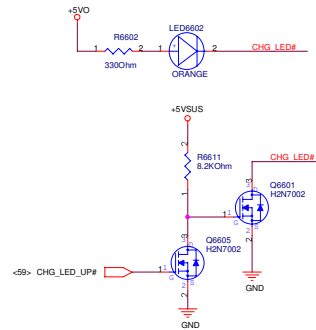


<Variant Name>

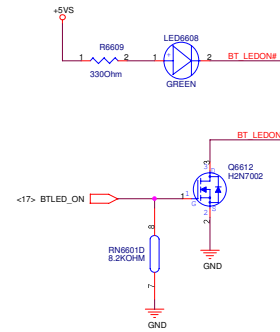
## For Power LED



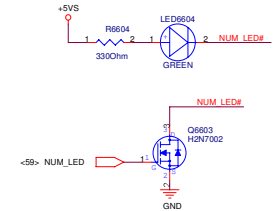
## For Battery LED



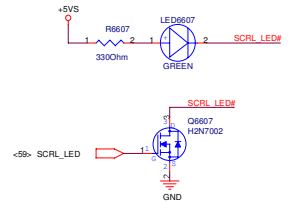
## For BT LED



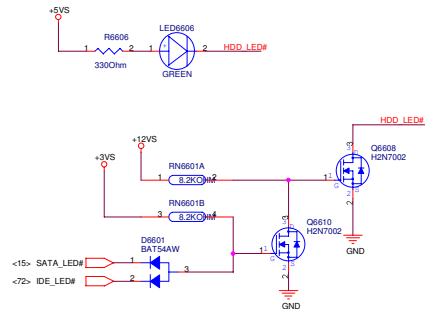
## For Number Lock



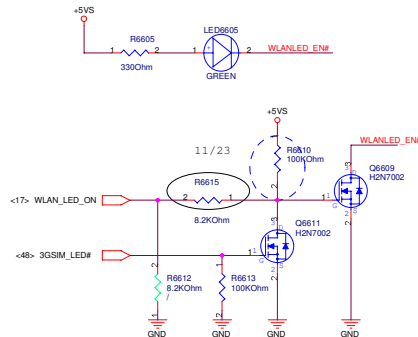
## For Scroll Lock



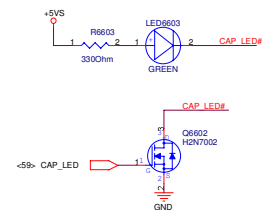
## For SATA/IDE LED

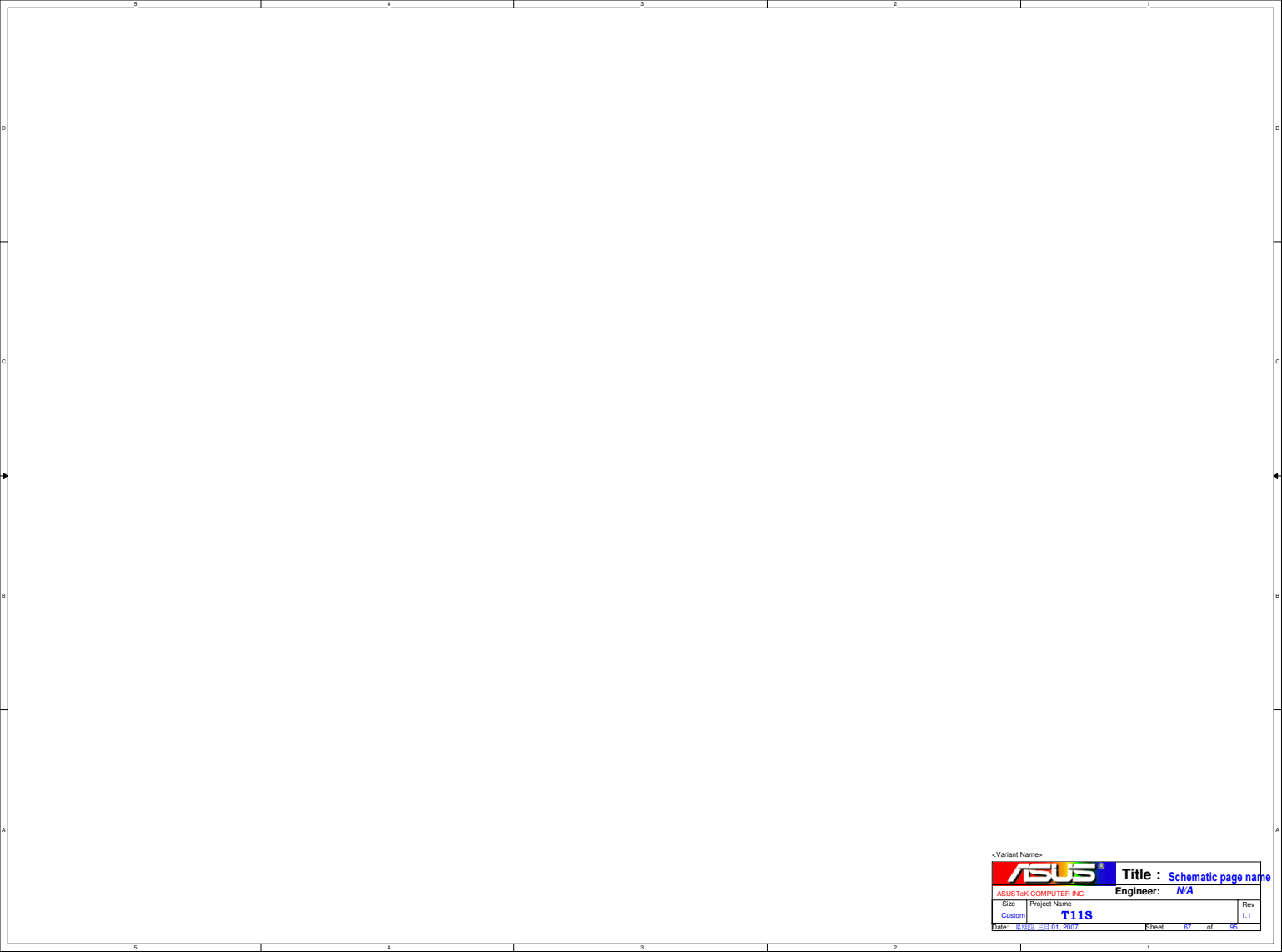


## For WireLess LED



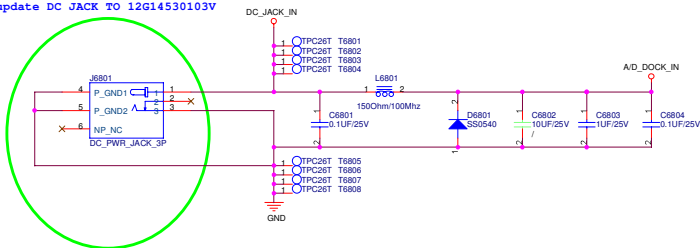
## For Caps. Lock



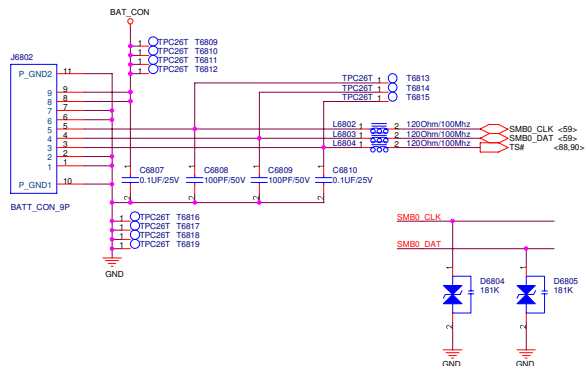


## DC IN

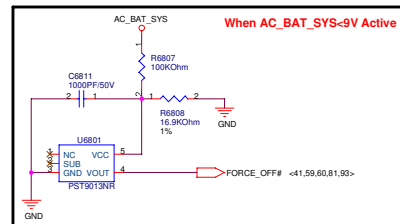
12/14 update DC JACK TO 12G14530103V



## BAT IN



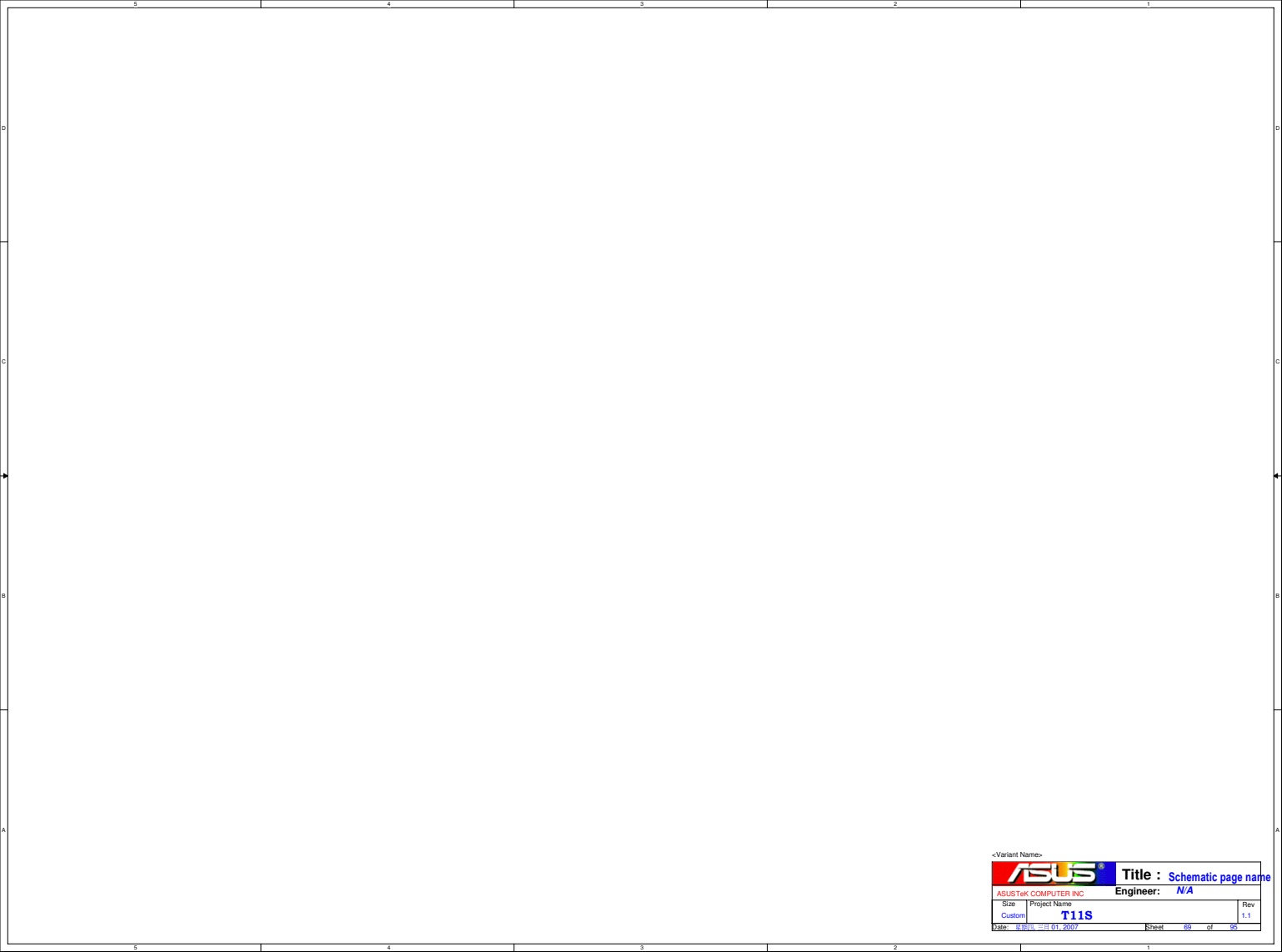
## Without Battery & Pull out Adapter



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<Variant Name>

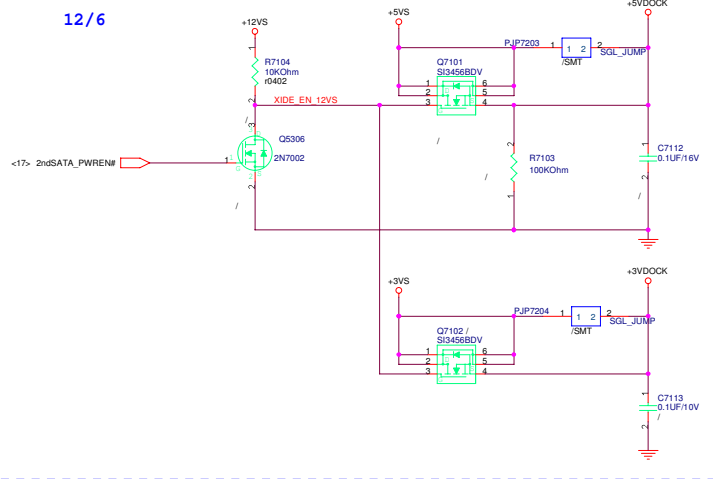
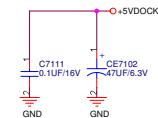
<b>ASUS</b>		<b>Title : DC &amp; BAT IN</b>	
ASUSTek COMPUTER INC. NB1		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 01/01/2007		Sheet 68 of 95	



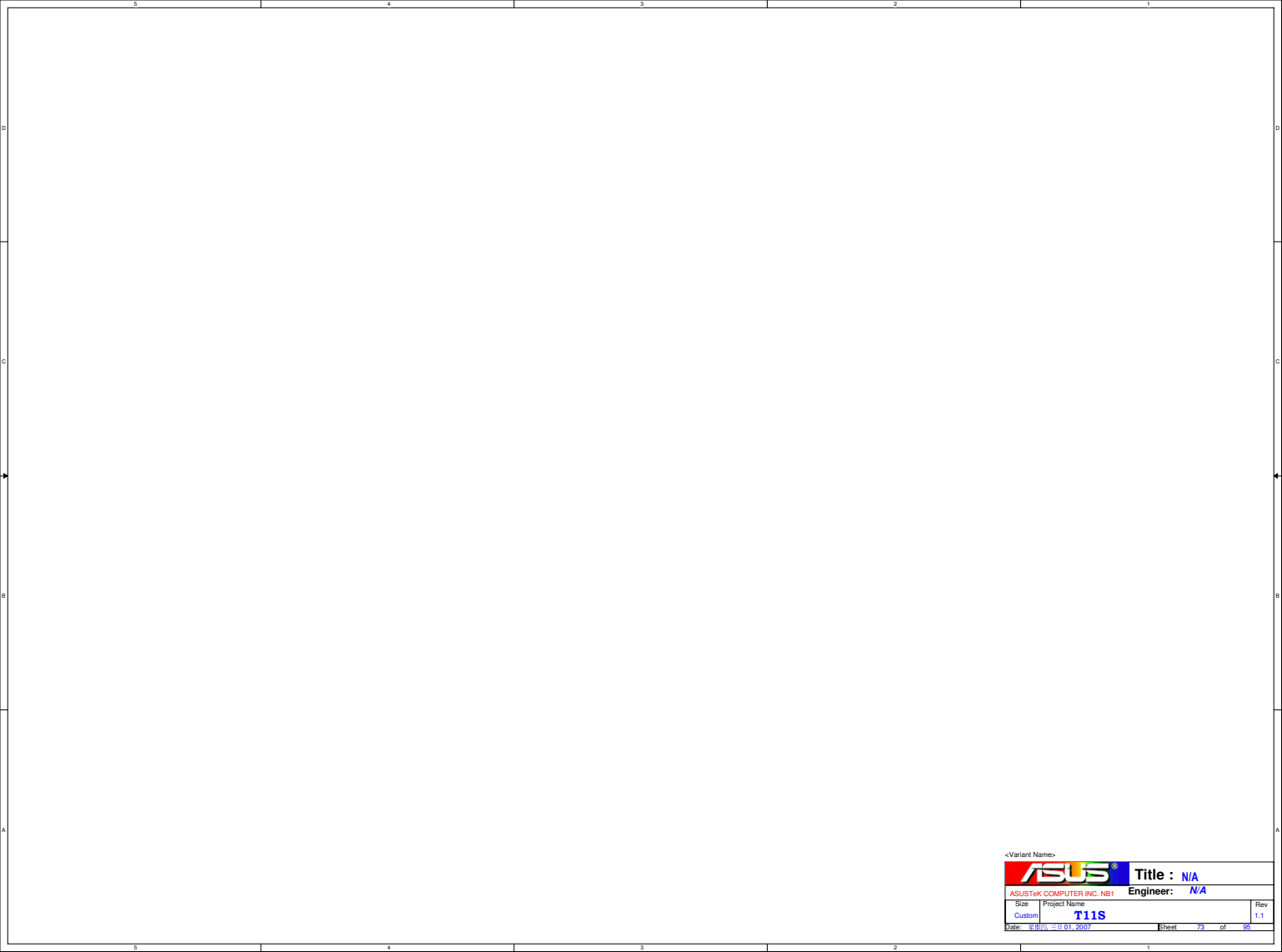
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		Title : Debug CONN.	
ASUSTeK COMPUTER INC		Engineer: N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 01/01/2007		Sheet	70 of 95

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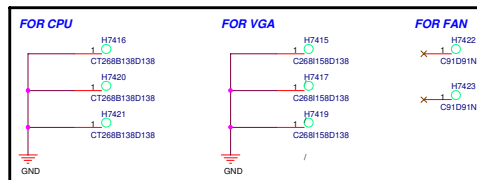
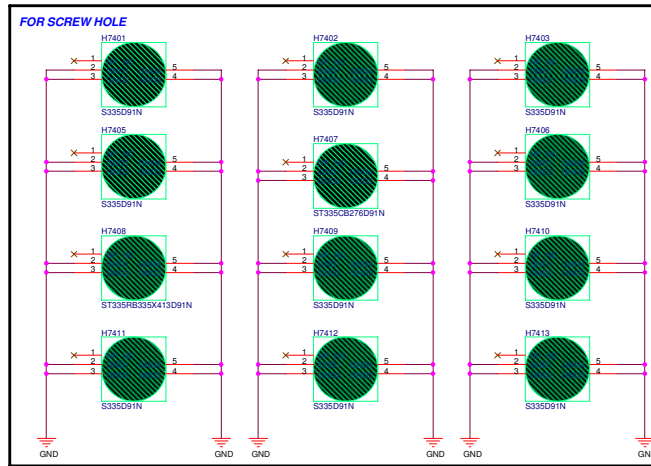
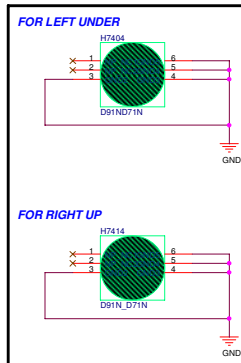
[illegible]

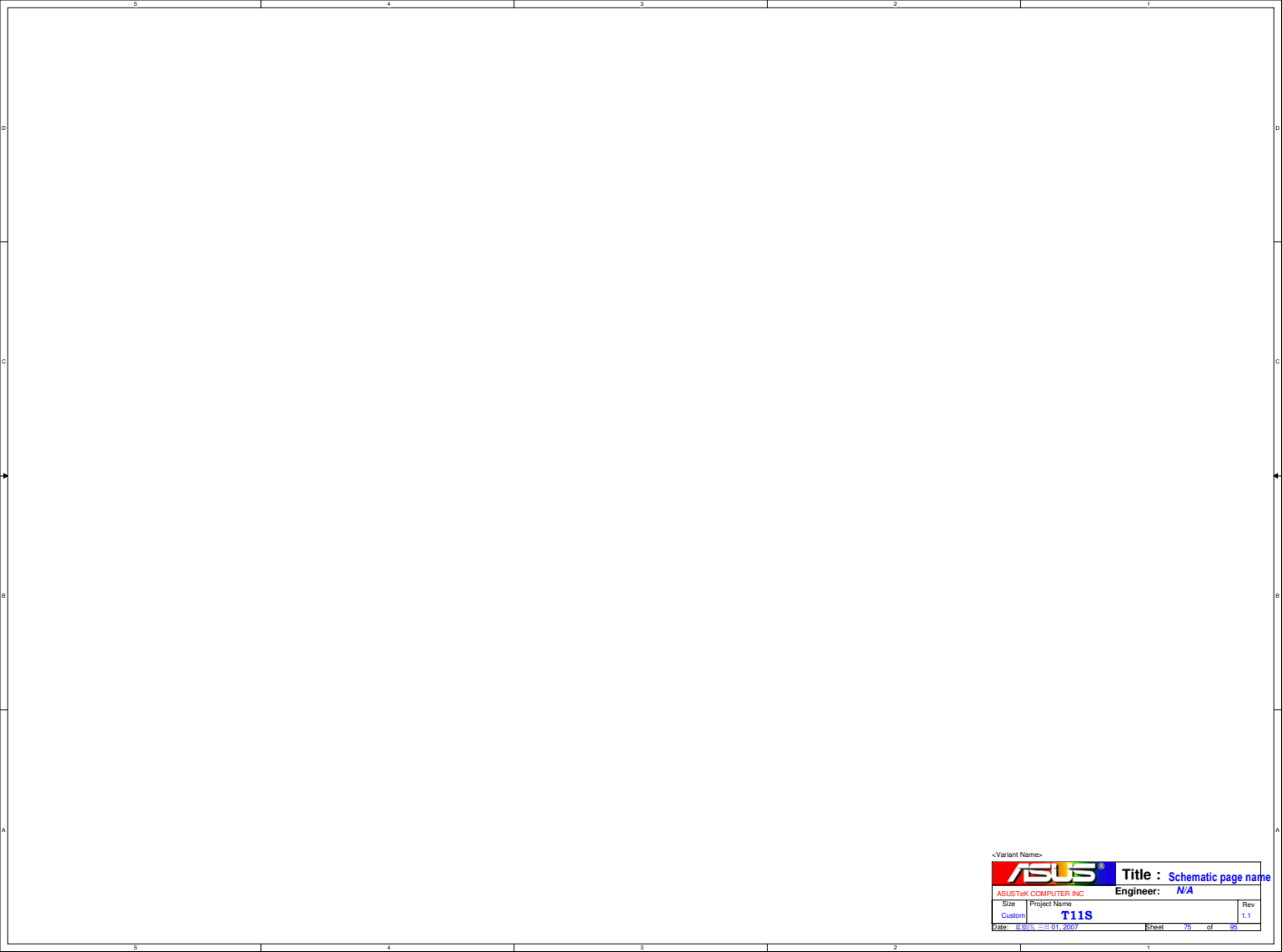





<Variant Name>

		Title : <b>N/A</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <b>N/A</b>	
Size	Project Name		Rev
Custom	<b>T11S</b>		1.1
Date: 01/01/2007		Sheet	79 of 95

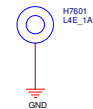
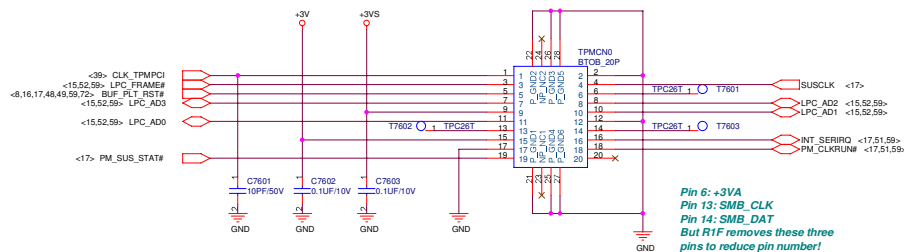


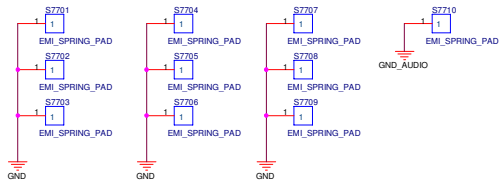


<Variant Name>

		<b>Title :</b> Schematic page name	
ASUSTeK COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 01/01/2007		Sheet 76 of 95	

# For TPM module

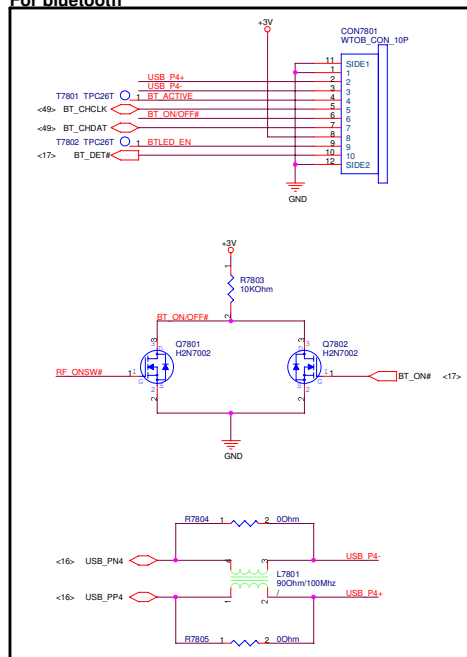




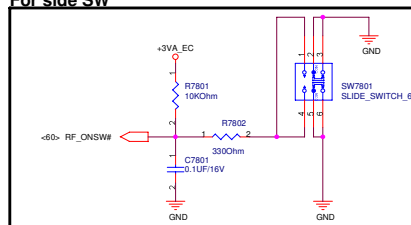
<Variant Name>

		<b>Title :</b> CIR	
ASUSTek COMPUTER INC		<b>Engineer:</b> N/A	
Size	Project Name		Rev
Custom	T11S		1.1
Date: 2007.01.01		Sheet	77 of 95

## For bluetooth

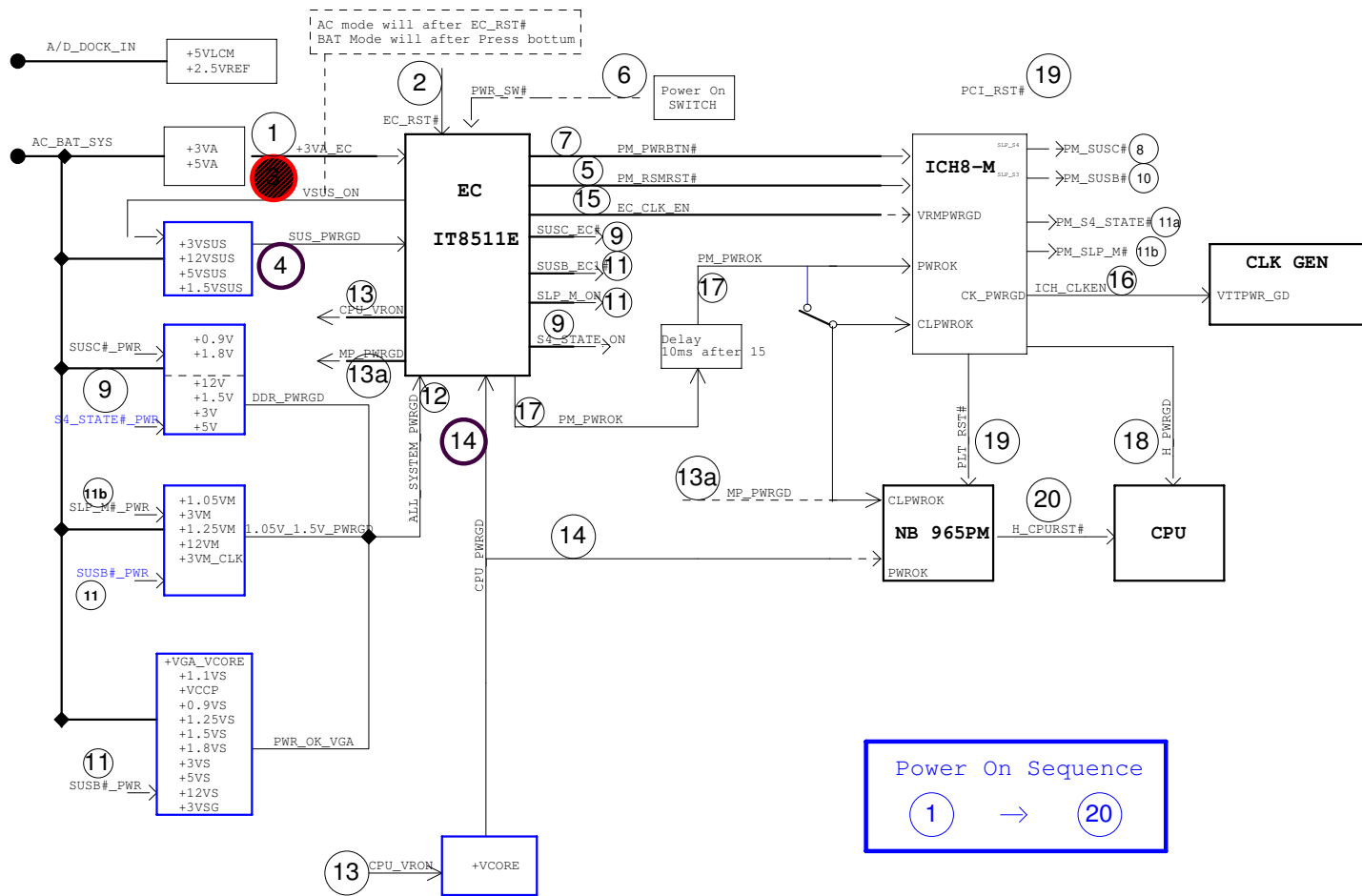


## For side SW

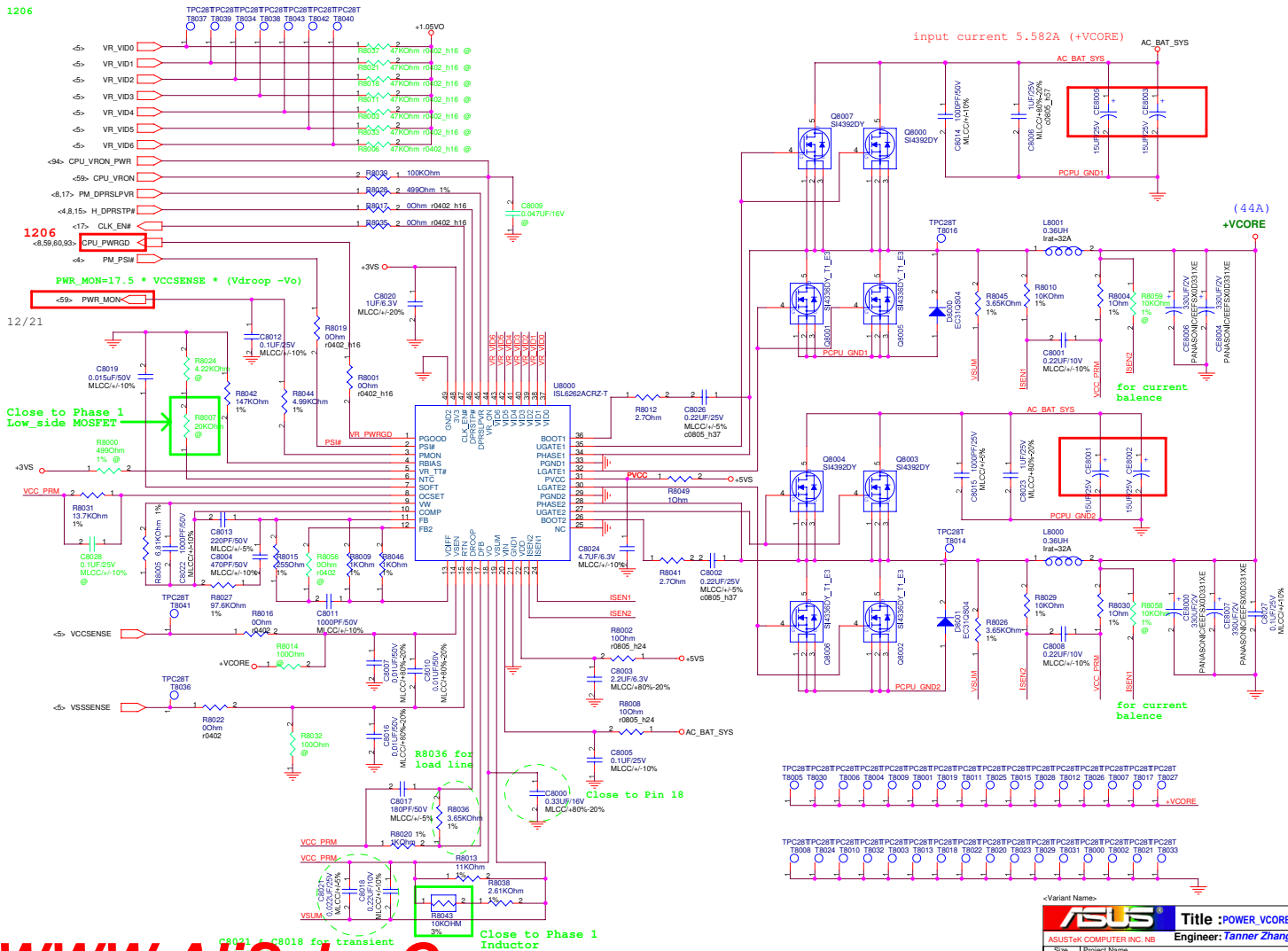


<Variant Name>

<b>ASUS</b>		<b>Title : Bluetooth</b>	
ASUSTek COMPUTER INC		Engineer: N/A	
Size	Project Name	Rev	
Custom	T11S	1.1	
Date: 01/01/2007	Sheet	76	of 95



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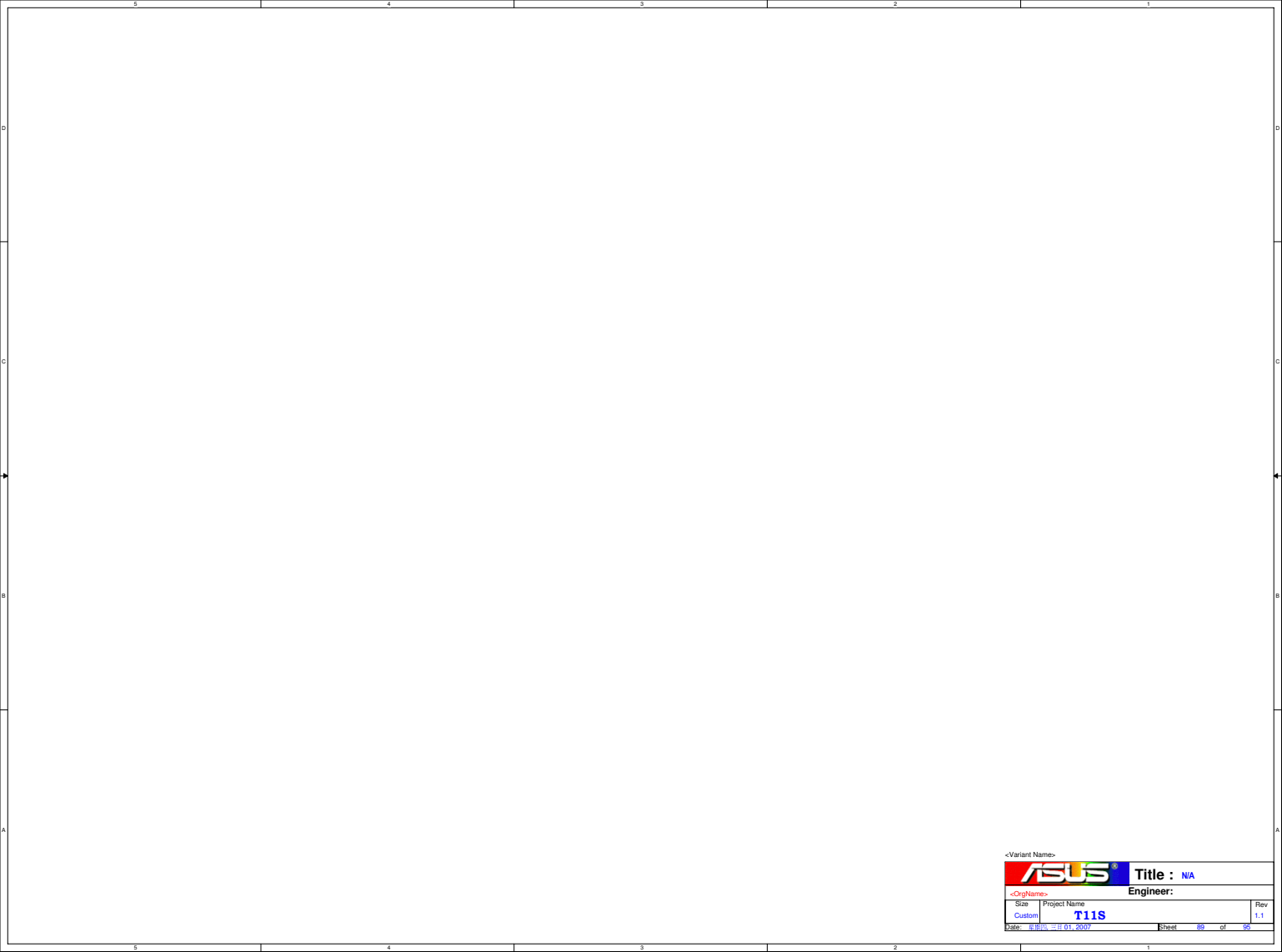
[illegible][illegible]




<Variant Name>		
		Title : NA
<OrgName>		
Size	Project Name	Rev
B	T11S	1.1
Date: 8/01/2007		Sheet 89 of 95







<Variant Name>



Title : **NA**

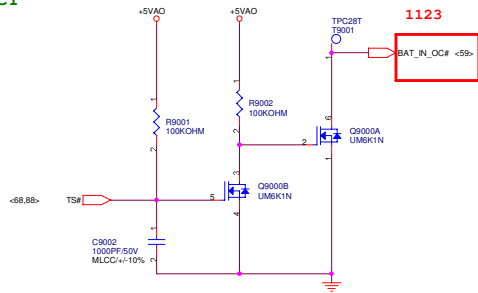
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Engineer:

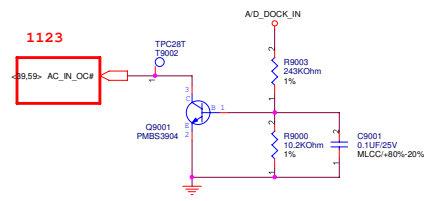
Size	Project Name	Rev
Custom	<b>T11S</b>	1.1

Date: 6/26/2007 8:01:20 AM Sheet 89 of 95

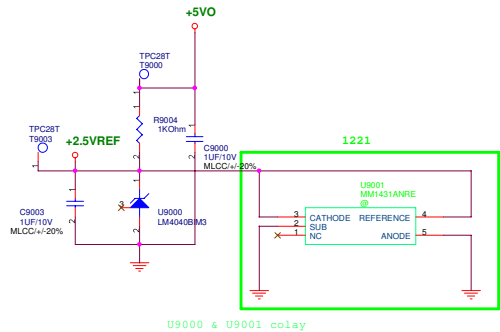
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



U9000 & U9001 colay



A/D\_DOCK\_IN

AC\_BAT\_SYS

V5US\_ON

MIC5235

+12VSUS  
(100mA)

SLP\_M#\_PWR

UMC4N  
(SWITCH)

+12VM

(10mA)

S4\_STATE#\_PWR

UMC4N  
(SWITCH)

+12V

(10mA)

SUSB#\_PWR

UMC4N  
(SWITCH)

+12VS

(10mA)

V5US\_ON

TPS51020

+3VO

S4\_STATE#\_PWR

PWM45EN

+3VSUS (0.473A)

SUSC#\_PWR

PWM45EN

+3V

(0.39A)

SUSB#\_PWR

FDW2501

+3VS

(3.128A)

SUSB#\_PWR

SI2304BDS

+3VAUX\_GOLAN (0.5A)

EC\_WLAN#\_PWR

SI2304BDS

+3VM

(1.06A)

SUSB#\_PWR

SI2304BDS

+3VSG

(0.726A)

SLP\_M#\_PWR

SI2304BDS

+3VM\_CLK

(0.25A)

V5US\_ON

FORCE\_OFF#

+5VO

S4\_STATE#\_PWR

FDW2501

+5VSUS

(0.5A)

SUSC#\_PWR

FDW2501

+5V

(2.8A)

+5VAO

+5VS

(4.376A)

+3VAO

+5VA

(0.1A)

--- SUS\_FWRGD

+3VA

(0.11A)

SI9183DT

SUSB#\_PWR

FDW2501

+1.5VS

(3.435A)

S4\_STATE#\_PWR

SI3456BDV

+1.5V

(0.4A)

SUSC#\_PWR

SI3456BDV

+1.5VSUS

(0.5A)

+1.05VO

+1.1VS

(1.1A)

CM8562

1.05V\_1.5V\_FWRGD

+1.05VM

(0.54A)

SI4336DY

SUSB#\_PWR

SI4336DY

+VCCP

(11.2A)

+5VO

SUSB#\_PWR

ISL6227

+1.5VO

+1.8V

(8.698A)

SUSC#\_PWR

MAX8632

+0.9VO

+1.8VS

(7.72A)

+5VO

S4\_STATE#\_PWR

SUSC#\_PWR

MAX8743

DDR\_FWRGD

+0.9V

(1A)

SUSB#\_PWR

FDW2501

+0.9VS

(1A)

SUSB#\_PWR

GPG\_VID

MAX8743

+VGA\_VCORE\_O

+VGA\_VCORE

(30A)

+5VO

SUSB#\_PWR

SLP\_M#\_PWR

MAX8743

+1.25VO

+1.25VM

(2A)

PWR\_OK\_VGA

+1.25VS

(1.5A)

SUSB#\_PWR

FDW2501

+5VS

CPU\_VRON

ISL6260C

+VGA\_VCORE\_O

+VGA\_VCORE

(44A)

VRM\_FWRGD, CLK\_EN#

+5VO

LM4040BIM  
(Regulator)

+2.5VREF

(10mA)

VR\_VID0-VR\_VID6, H\_DPRSTP#,  
MCH\_OK, PML\_DP6SLPWR, PML\_PS1#,  
PML\_DP6SLPWR, PML\_PS1#,  
PML\_DP6SLPWR, PML\_PS1#

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<Variant Name>

ASUS

Title : POWER\_VCORE

<OrigName>

Engineer: Tanner Zhang

Size Project Name

Custom T11S

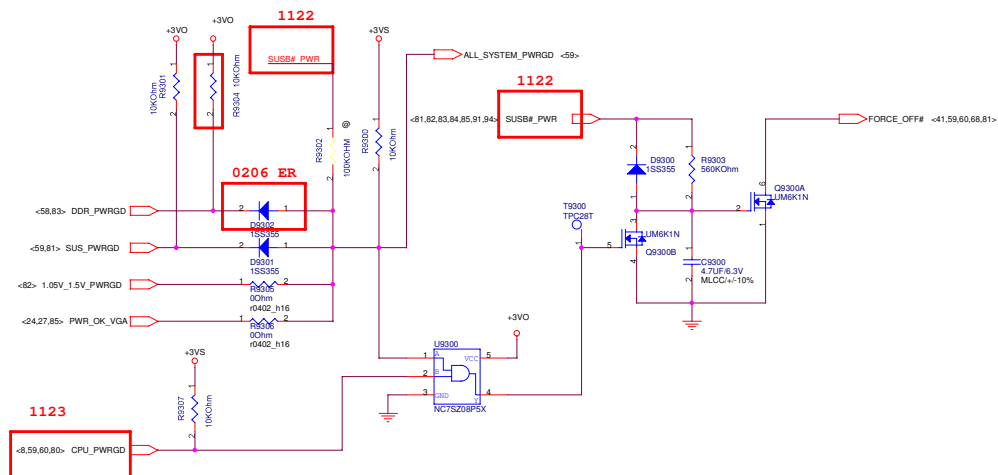
Date: 2011-11-31 2011

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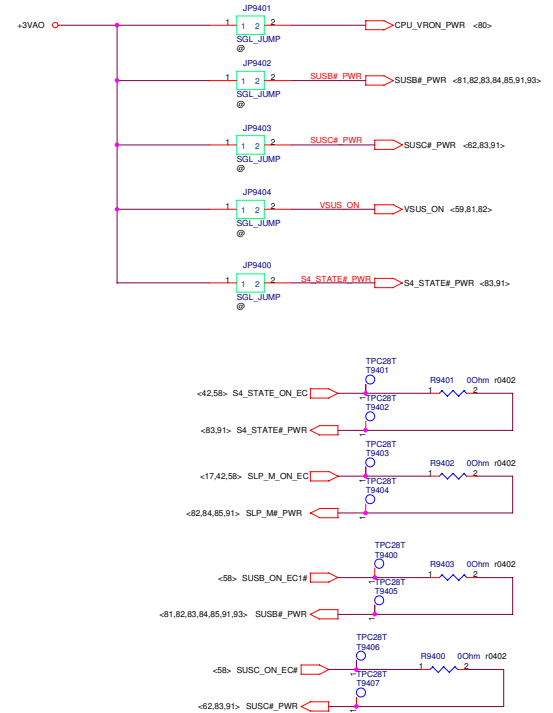
Rev

1.1

## POWER GOOD DETECTOR



# FOR POWER TEST



Rev	Date	Description
1.0	2006/11/	1. Initial release.
1.1	2007/02/09	1.WLAN_ON#(GPIO17) change to +3VS pull High (page 17) 2.R5950,R5920 delle,Delete Q3901,Q3902 (page 59,39) 3.D6201 5pin power 改在bead 后 (page 62 layout request) 4.Delete D5102 (page 51) 5.82566mm errata:add 10nf between +3V and 1.8vctrl and +1.0Vctrl (page 44) 6.R2460,R2422,R2426 unstuff,R2323 pull Down (page 23,24) 7.Add C2003,CN2201,CN2202,CN2206 (page 20,22) 8.SPI ROM P/N change to:05G001405010 (page 65) 9.ADD +3VM&+1.05VM POWER OK SIGNAL add H/W optional MP_PWRGD & LAN_RST# ciucuit.(page 58) 10.modify the Keyboard Matrix (page 61) 11.add GPU VID control 1(page 24) 12.SB GPIO12 change from "EXT_SCI"# to "LAN_PHYPC" for AMT (page 17) optional 13.Change C2940 to0.1uF.[28] 14.R1761 LAN_WOL_EN Pull high to +3VSUS Optional (page 17) 15.R3952 change to 270 ohm 1% (page 39) 16.delete LPC debug circuit(page 70) 17.unstuff the +1.05VM discharge circuit.(page 42)

Rev	Date	Description

<Variant Name>

		Title : <a href="#">History</a>	
ASUSTek COMPUTER INC		Engineer: <a href="#">N/A</a>	
Size Custom	Project Name <b>T11S</b>	Rev 1.1	
Date: 07/02/2007		Sheet 95 of 95	